NoCs: Past, Present and Future

Giovanni De Micheli

EPFL
NoCs: Connecting people

SPIN: a Scalable, Packet Switched, On-chip Micro-network

Adrijean Adriahtenaina (UPMC/LIP6)
Hervé Charley (UPMC/LIP6)

Networks on Chips:
A New SoC Paradigm

Æthereal Network on Chip:
Concepts, Architectures, and Implementations

Kees Goossens, John Dielissen, and Andrei Rădulescu
Philips Research Laboratories
NoCs: Connecting design

- Connecting scientific communities
  - Multiprocessor Design, Communication, EDA

- Connecting technologies
  - Silicon, optical, RF

- Providing hardware scalability through raising design abstraction level
The Rise of Networks-on-Chip

Chip for mobile multimedia apps (under NDA)
The Network-on-Chip Paradigm

The “power of NoCs”:

- **Clean separation** at session layer
  - Cores issue end-to-end transactions
  - Network deals with transport, network, link, physical

- **Modularity** at HW level: only 2 building blocks
  - Network interface
  - Switch (router)

- **Physical design aware** (floorplan global routing)

**Scalability is supported from the ground up!**
NoCs: Past and Present
Enabling multiprocessing

Technology
65nm CMOS Process

Interconnect
1 poly, 8 metal (Cu)

Transistors
100 Million

Die Area
275 mm²

Tile Area
3 mm²

Package
1248 pin LGA, 14 layers, 343 signal pins
Enabling multiprocessing

Apple A11 SoC

<table>
<thead>
<tr>
<th>Technology</th>
<th>10nm CMOS Process TSMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor</td>
<td>ARM v8A 6-core</td>
</tr>
<tr>
<td>Transistors</td>
<td>4.3 Billion</td>
</tr>
<tr>
<td>Die Area</td>
<td>88 mm²</td>
</tr>
<tr>
<td>Application</td>
<td>mobile</td>
</tr>
<tr>
<td>Package</td>
<td>Package on Package With 2GB of memory</td>
</tr>
</tbody>
</table>
NoCs: Enabled by EDA

- From academic startups
NoCs: Enabled by EDA

- To market leaders: Arteris
The Future

- Almost all telephones and cars have a NoC