Call for Papers

11th IEEE/ACM International Symposium on Networks-on-Chip
October 19 – 20, 2017
Seoul, South Korea
(Co-located with Embedded Systems Week 2017)

*** EXTENDED DEADLINE: Abstract May 8th, Full paper: May 15th ***

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to
interdisciplinary research on on-chip, chip-scale, and multichip package scale communication
technology, architecture, design methods, applications and systems. NOCS brings together scientists
and engineers working on NoC innovations and applications from inter-related research communities,
including computer architecture, networking, circuits and systems, packaging, embedded systems, and
design automation. Topics of interest include, but are not limited to:

+ NoC Architecture and Implementation
  – Network architecture (topology, routing, arbitration)
  – NoC Quality of Service
  – Timing, synchronous/asynchronous communication
  – NoC reliability issues
  – Network interface issues
  – NoC design methodologies and tools
  – Signaling & circuit design for NoC links

+ NoC Analysis and Verification
  – Power, energy & thermal issues (at the NoC, un-core and/or system-level)
  – Benchmarking & experience with NoC-based hardware
  – Modeling, simulation, and synthesis of NoCs
  – Verification, debug & test of NoCs
  – Metrics and benchmarks for NoCs

+ Novel NoC Technologies
  – New physical interconnect technologies, e.g., carbon nanotubes, wireless NoCs, through-silicon, etc.
  – NoCs for 3D and 2.5D packages
  – Package-specific NoC design
  – Optical, RF, & emerging technologies for on-chip/in-package interconnects
  – In-memory network and NoCs for new memory technologies

+ NoC Application

- Mapping of applications onto NoCs
  - NoC case studies, application-specific NoC design
  - NoCs for FPGAs, structured ASICs, CMPs and MPSoCs
  - NoC designs for heterogeneous systems, fused CPU-GPU
architectures, etc
  - Scalable modeling of NoCs

+ NoC at the Un-Core and System-level
  - Design of memory subsystem (un-core) including memory controllers,
caches, cache coherence protocols in NoCs
  - NoC support for memory and cache access
  - OS support for NoCs
  - Programming models including shared memory, message passing and
novel programming models
  - Issues related to large-scale systems (datacenters,
supercomputers) with NoC-based systems as building blocks

+ On-Chip Communication Optimization
  - Communication efficient algorithms
  - Communication workload characterization & evaluation
  - Energy efficient NoCs and energy minimization

+ Off-Chip and Rack-Level Communication
  - All aspects of inter-chip network design
  - All aspects of rack-level network design

Electronic paper submission requires a full paper, up to 8 double-
column IEEE format pages,
including figures and references. The program committee in a double-
blind review process will
evaluate papers based on scientific merit, innovation, relevance, and
presentation. Submitted
papers must describe original work that has not been published before
or is under review by another
conference or journal at the same time. Each submission will be
checked for any significant
similarity to previously published works or for simultaneous
submission to other archival venues,
and such papers will be rejected. Proposals for special sessions and
demos are invited. Paper
submissions and demo proposals by industry researchers or engineers to
share their experiences and
perspectives are also welcome. Please find the detailed submission
instructions for paper
submissions, special session, and demo proposals at the submission
page. Further information is
available via: http://www.arc.ics.keio.ac.jp/nocs17/

Important Dates

   Abstract registration deadline May 8th, 2017
   Full paper submission deadline May 15th, 2017
   Notification of acceptance   July 1st, 2017
   Final version due   August 1st, 2017

General Co-Chairs:
   Axel Jantsch (Vienna University of Technology, Austria)
   Hiroki Matsutani (Keio University, Japan)

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