**XNoTs: Crossbar-Connected Multi-Layer Topologies for 3-D NoCs**

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3-D Network-on-Chips: several small-sized wafers are connected with through-wafer vias (high-speed & density)

Long wire delay!

3-D IC

2-D IC

3-D IC (4-tier)

L mm

L/2 mm

3D-Mesh is used in 3-D NoCs (narrow range of choice)

3-D Mesh (top view)

3-D Torus (side view)

XNoTs for 3-D NoCs: vertically-arranged routers and cores are tightly coupled with a single crossbar switch

Examples: each tier can be independently customized

X-mesh (mesh-based)

X-ft (tree-based)

XNoTs (top view)

XNoTs (side view)
Deadlock-free routing for XNoTs:
1) Intra-tier transfer: use existing routing on each tier
2) Inter-tier transfer: prohibit turns from a lower-numbered tier to a higher-numbered tier

Average hop count of XNoTs is shorter than 3-D mesh/torus, because of inter-tier crossbar switches

Throughput of XNoTs is comparable to 3D-mesh/torus

Summary: XNoTs for 3-D NoCs
1) Various types of XNoTs (mesh- & tree-based) can be created
2) Better average hop count, and comparable throughput
3) Smaller network logic area, and less energy consumption