Near-Field Coupling Integration Technology

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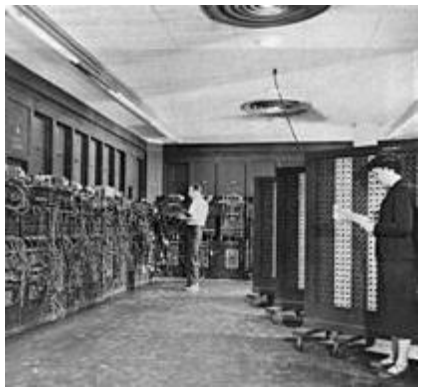
Challenge to “Tyranny of Numbers”

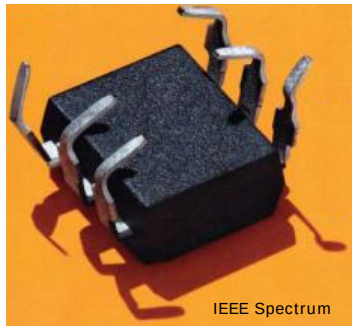


ENIAC
1946
17 thousand vacuum tubes,
5 million hand-soldered connections

Cray-3
1993
Mass of wires, cables,
and connectors

K
2011
200 thousand cables,
1,000Km long

From
“System on a Chip”
to
“System on Chips”



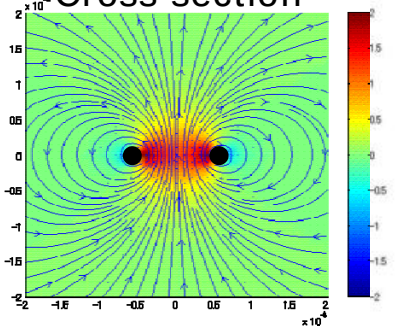
Invention of transistor (1948), IC (1958) → End of Moore’s Law

- Invention of IC driven by “Tyranny of Numbers”:
  Challenges implied by large number of components & interconnects.
- We face the same challenge again with end of Moore’s Law
  and rise of IoT/big data.

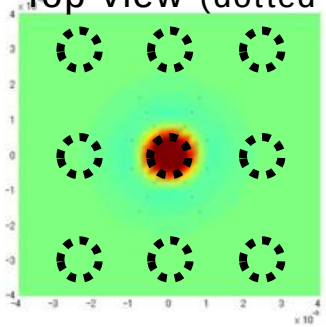
Proposal: Near-Field Coupling

- Replace mechanical connections (wires, solders, connectors) by electrical ones (wireless by near-field coupling).
- Near-field coupling provides with invisible wires.
  - Near Field (Reactive)

Cross section



Top view (dotted circles: coils)



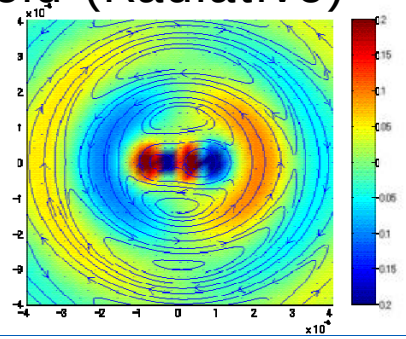
Near Field : $x < \lambda/2\pi$

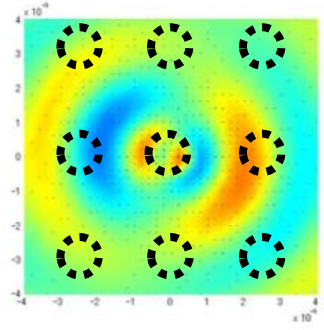
x: distance, λ: wave length

$V_{RX} \propto 1/x^3$ (-60dB/dec)

Smart cards used in place of train ticket, door key

  - Far Field (Radiative)

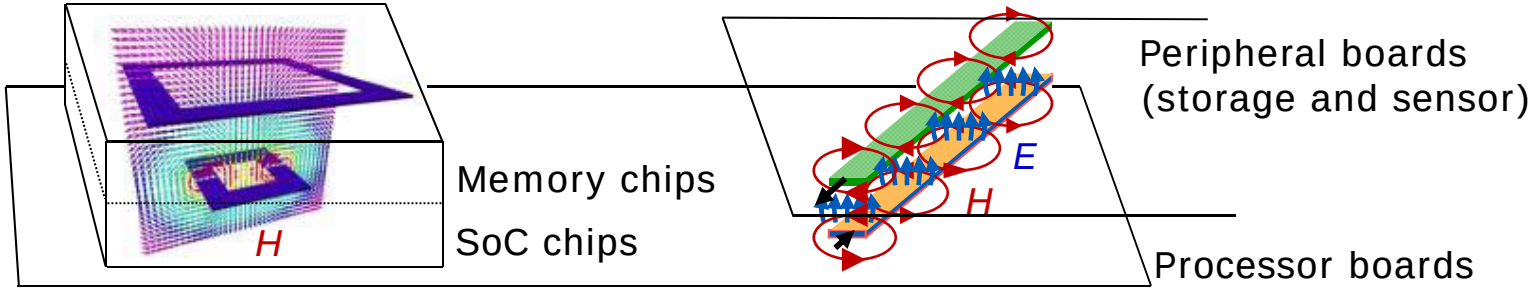




WiFi, Cellular

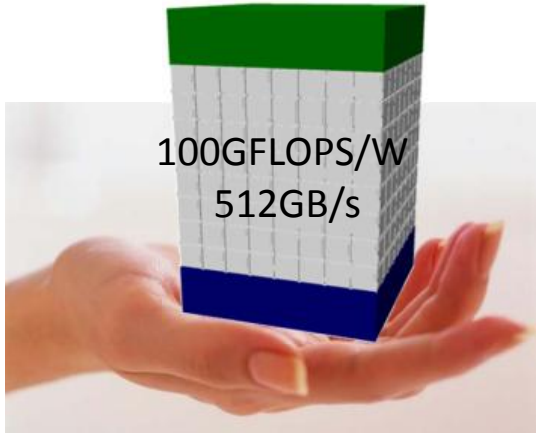
Near-Field Coupling Integration Technology

- Proposed solution to “connections in very large system”



ThruChip Interface (TCI)
3D integration of chips
for high performance

Transmission Line Coupler (TLC)
LEGO-type packaging of modules
for high function



JST ACCEL Project (2015-2019):

Data Centric Computer
(Ultra low power mobile computer in the era of IoT)

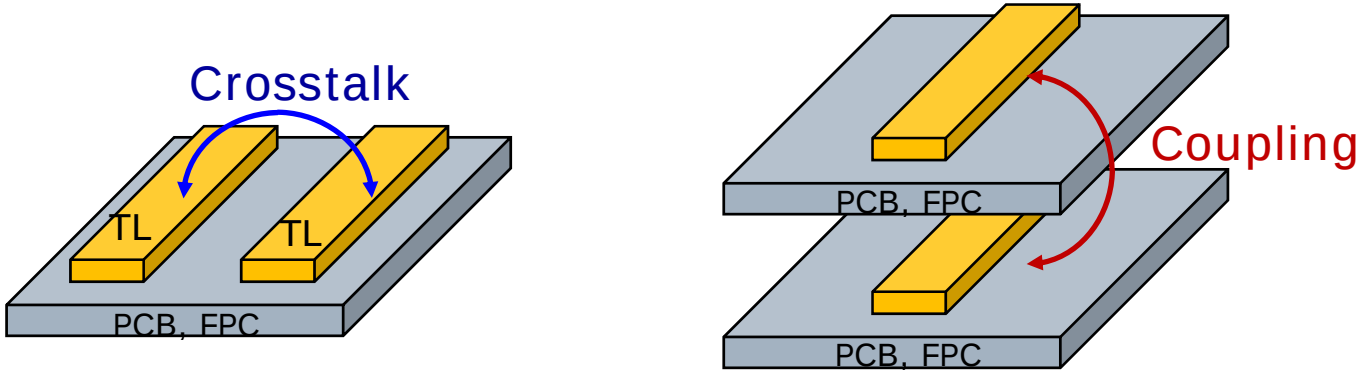
Proof of Concept: 100GFLOPS/W (in 2019)

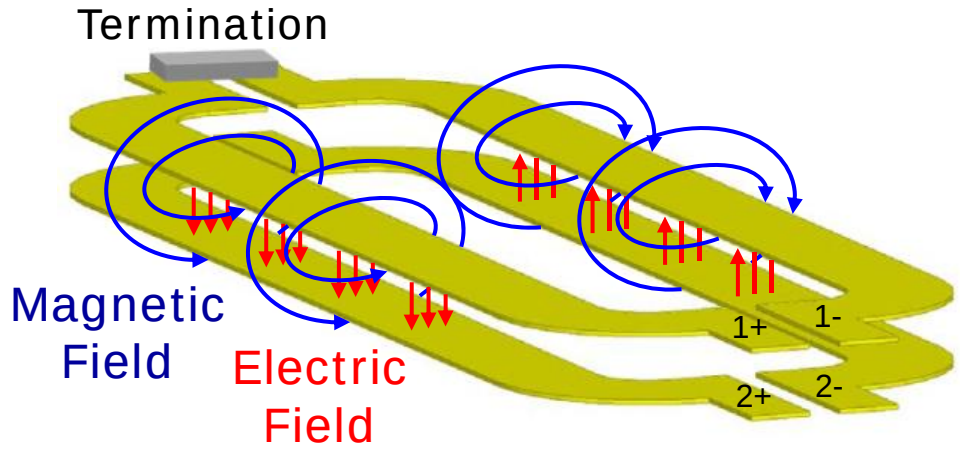
Milestone: 512GB/s 8GB DRAM (in 2017)

Outline

- Near-Field Coupling Integration Technology
- Transmission Line Coupler (TLC)
- ThruChip Interface (TCI)
- Challenges
  - Highly Doped Silicon Vias (HDSV)
  - TCI_2.9D/2.5D/2.0D
- ACCEL
  - 100GFLOPS/W Computer and 512GB/s DRAM

Transmission Line Coupler (TLC)





Transmission Line Coupler (TLC)

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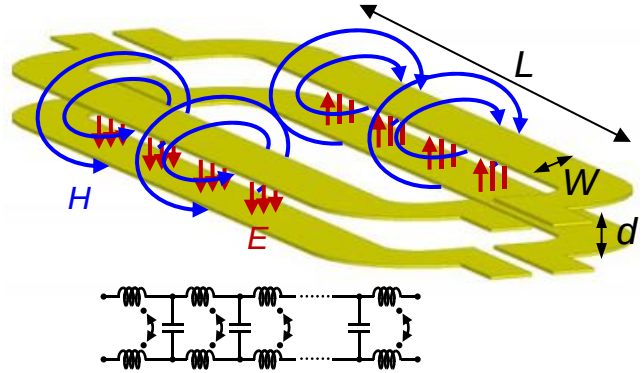
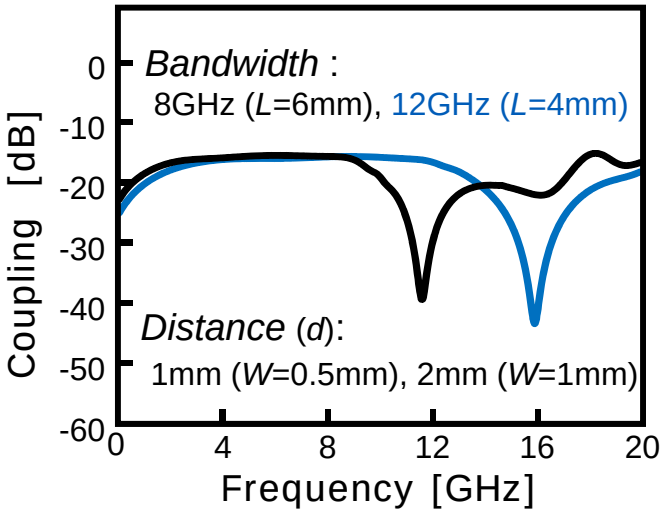


distributed system

- Electromagnetic coupling
  - characteristic impedance is controlled
  - signal reflection can be suppressed
- Transceiver: digital CMOS circuits
- Contactless connector
- Modular design

ISSCC2011, pp.492-493

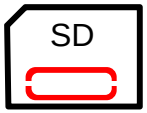


Video 1

Video 2

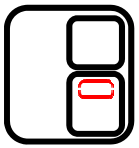
http://www.kuroda.elec.keio.ac.jp/research/video/

Applications of TLC

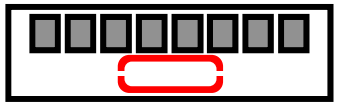


Memory Card
High-speed：50x（12Gb/s）
Low-power：1/500
Water proof
(pad-less, sealed)
ISSCC2013 , pp.214-215

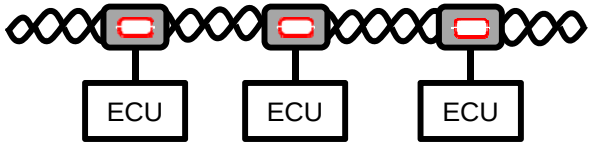
Display
High-speed：10x（6Gb/s）
Low-energy：1/10（16pJ/b）
Thin
（no mechanical structure）
ISSCC2013, pp.200-201



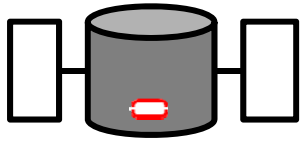
Smartphone
High-speed ：5x（6Gb/s）
Low-energy ：1/24（6pJ/b）
Modular design
(electrical connection)
ISSCC2015 , pp.176-177



DIMM
High speed：5x（12.5Gb/s）
Multi-drop bus
(impedance controlled)
ISSCC2012 , pp.52-53



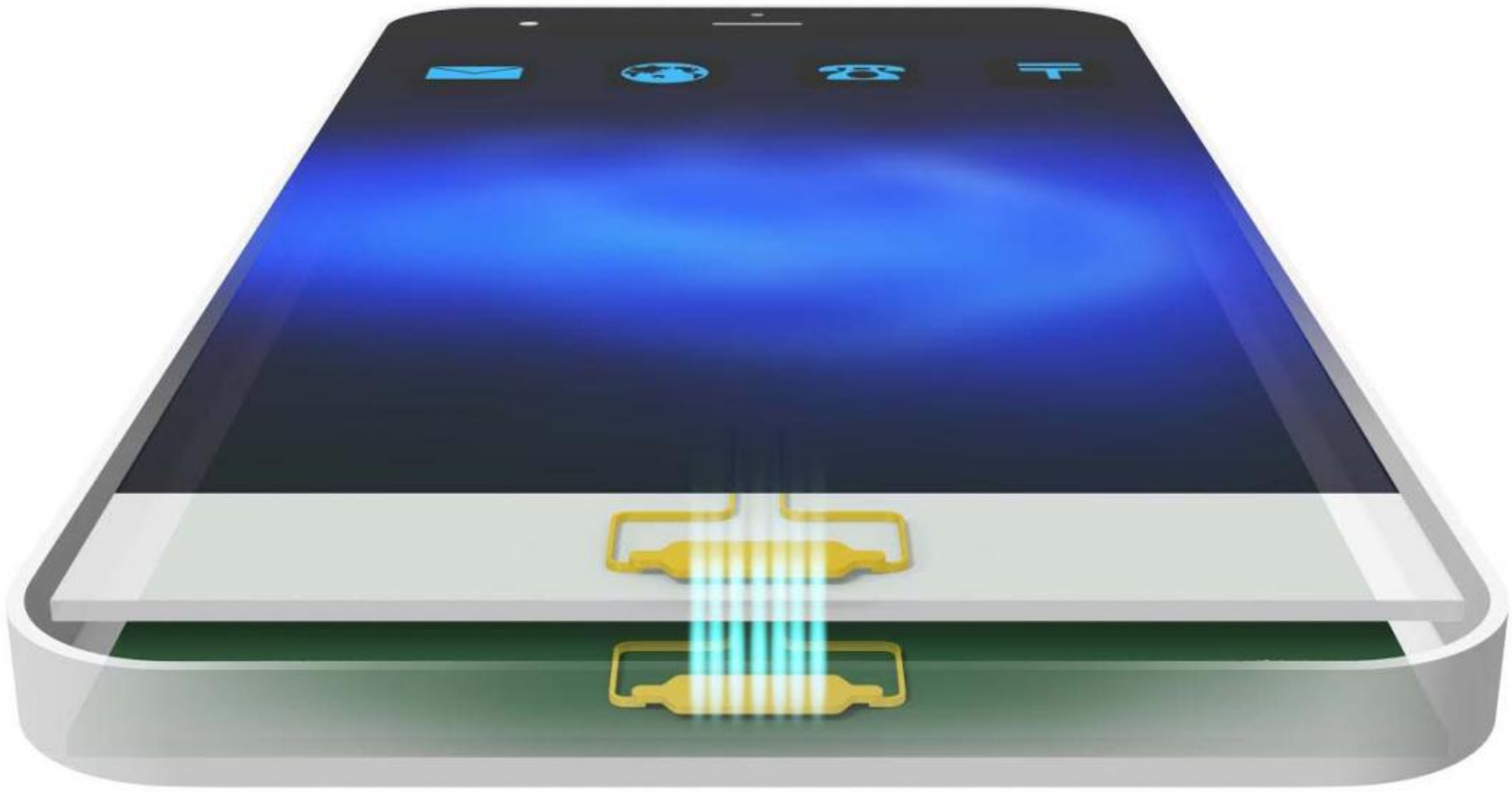
In-vehicle LAN
Light: 30%
Strong EMC immunity
(wide band)
ISSCC2014 , pp.496-497



Satellite
Light: 60%
Vibration immunity
(contactless connection)
ISSCC2015 , pp.434-435

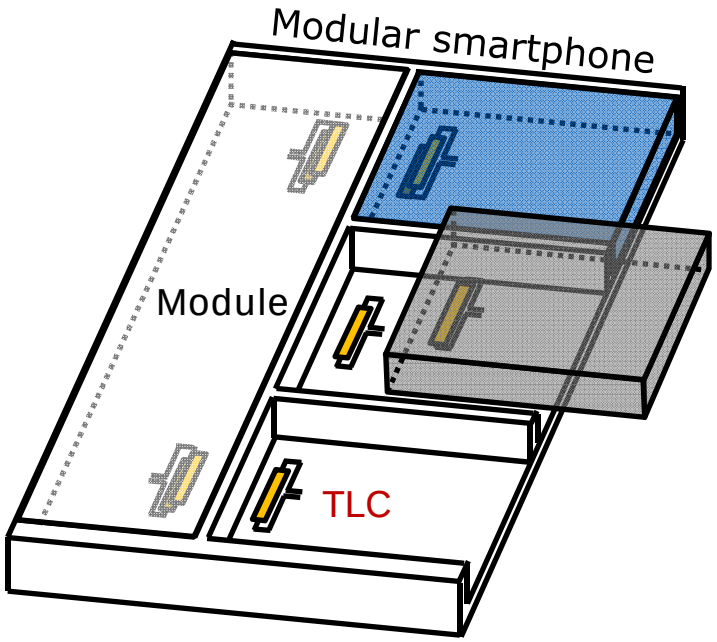
Display/Camera Module

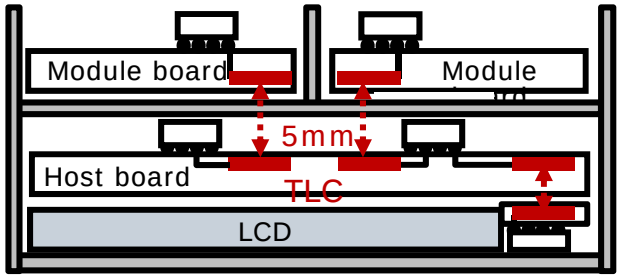
- High speed, Low power, Low profile



ISSCC2013, pp.200-201

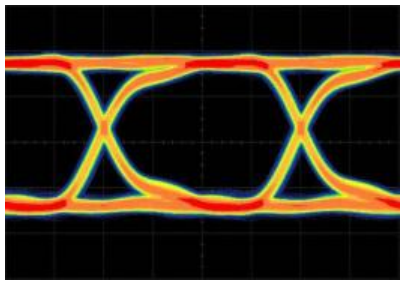
Modular Design

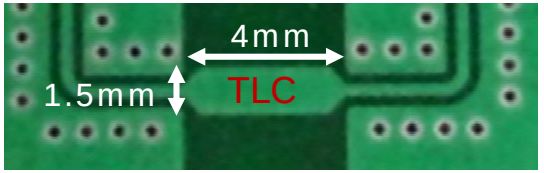




ISSCC2015, pp.176-177

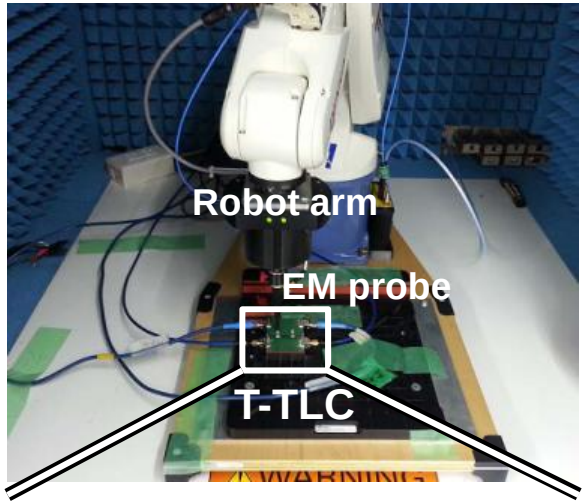
6Gb/s received data

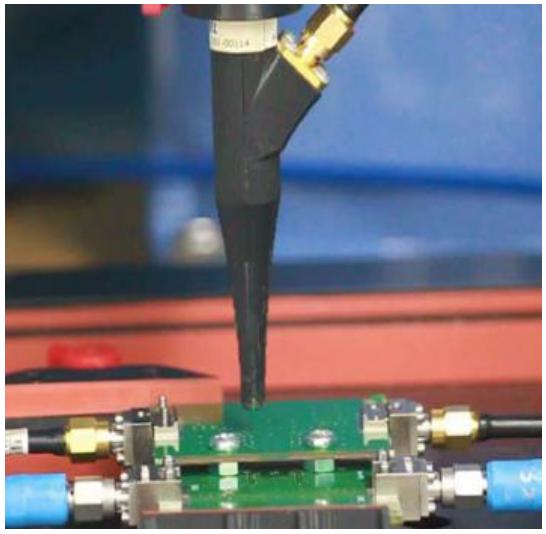




Video 3
http://www.kuroda.elec.keio.ac.jp/research/video/

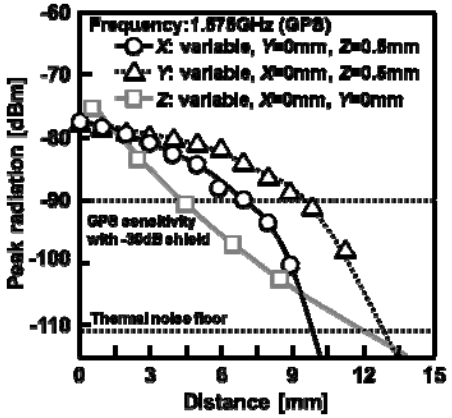
Radiation Tolerance (EMC)

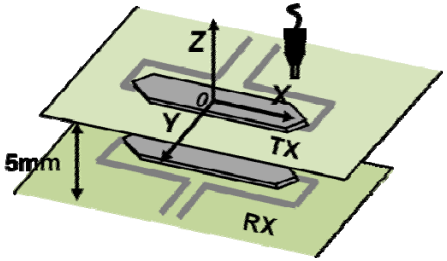




1) EMI: Electromagnetic Interference

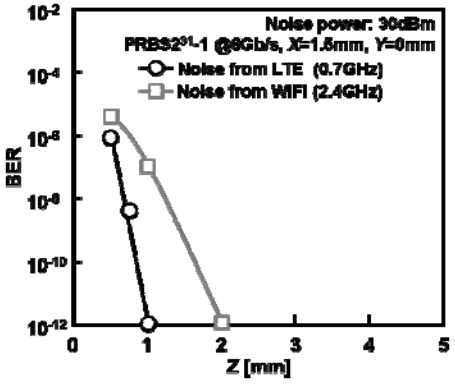
GPS is not affected at a separation of 10mm from TLC

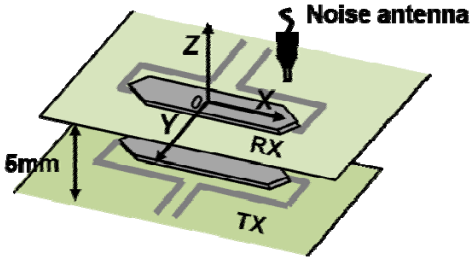




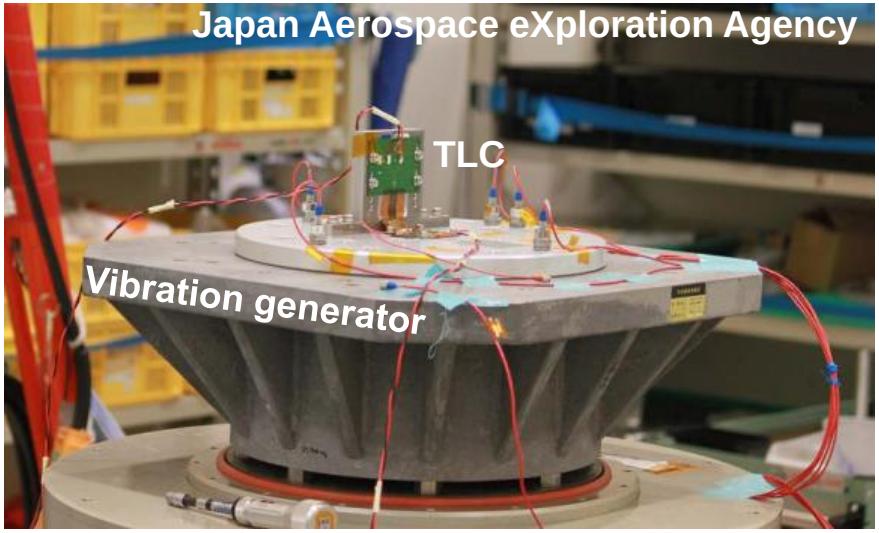
2) EMS: Electromagnetic Susceptibility

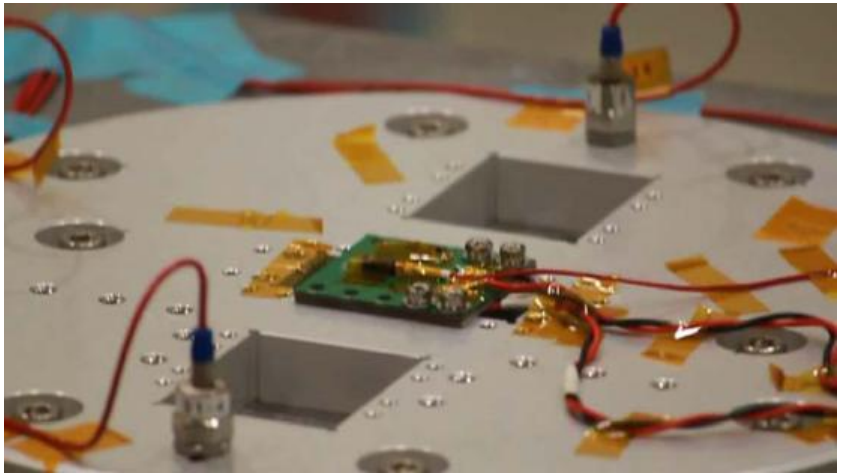
TLC is not affected at a separation of 2mm from LTE/WiFi



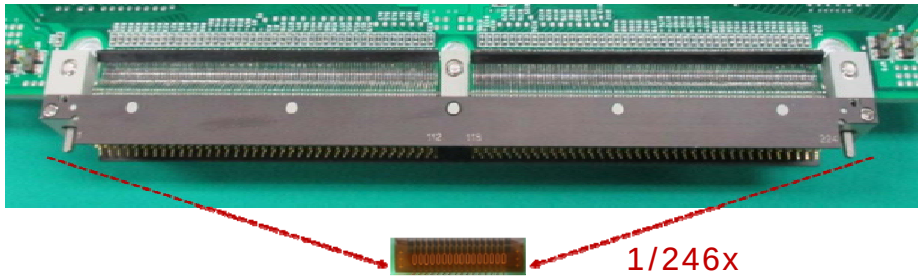


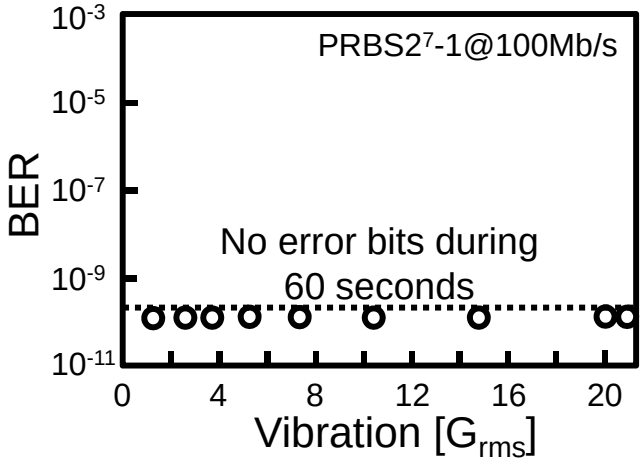
Vibration Tolerance





Conventional mechanical connector

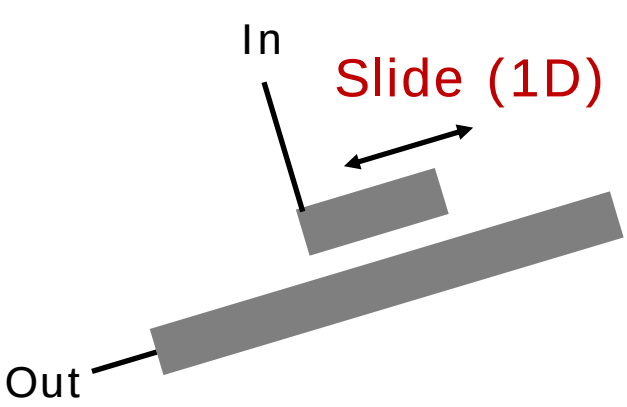




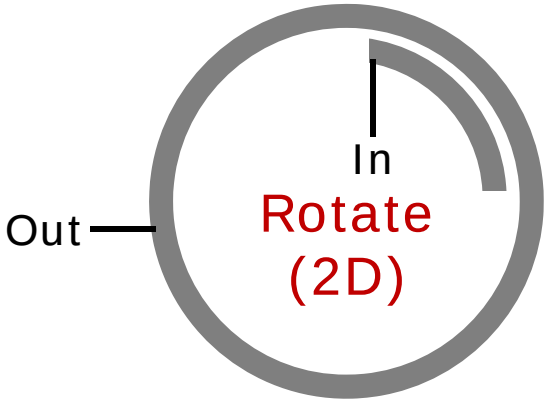
No single bit failure during the period of launch of small locket

ISSCC2015 , pp.434-435

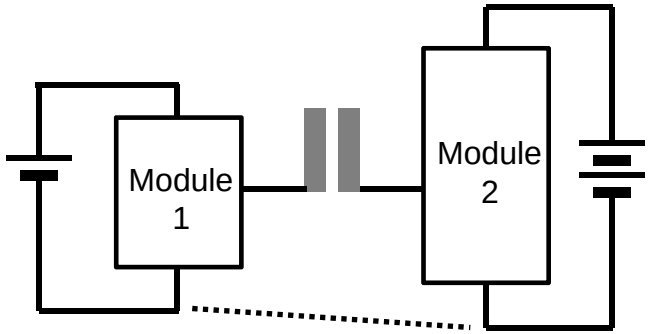
Other Possibilities



door, seat



wheel, joint ...



DC isolation

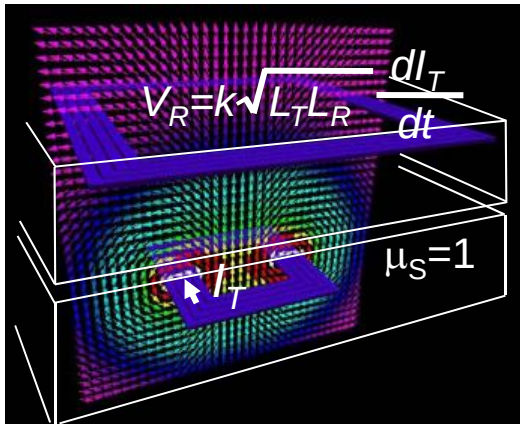
Video 4

Touch and Go
Hot swap

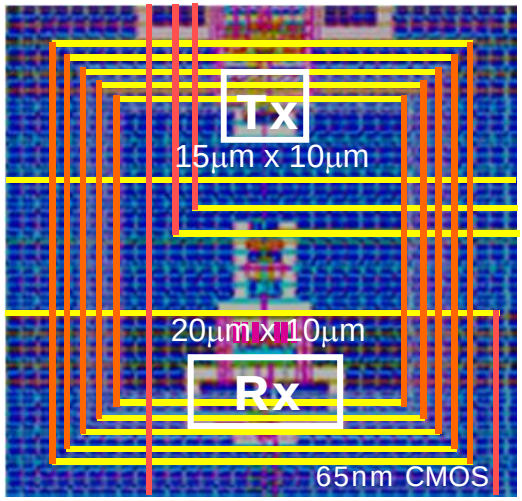
Outline

- Near-Field Coupling Integration Technology
- Transmission Line Coupler (TLC)
- ThruChip Interface (TCI)
- Challenges
  - Highly Doped Silicon Vias (HDSV)
  - TCI_2.9D/2.5D/2.0D
- ACCEL
  - 100GFLOPS/W Computer and 512GB/s DRAM

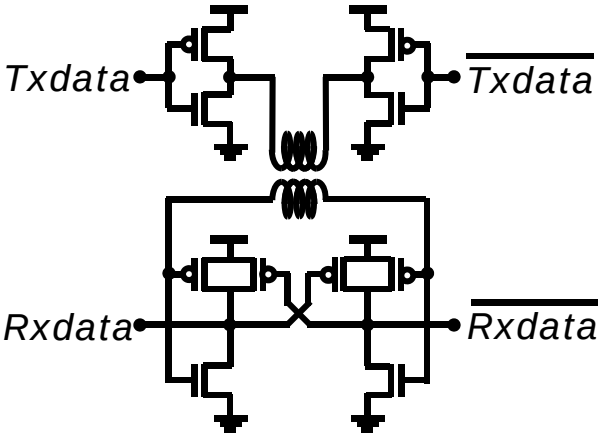
ThruChip Interface (TCI)

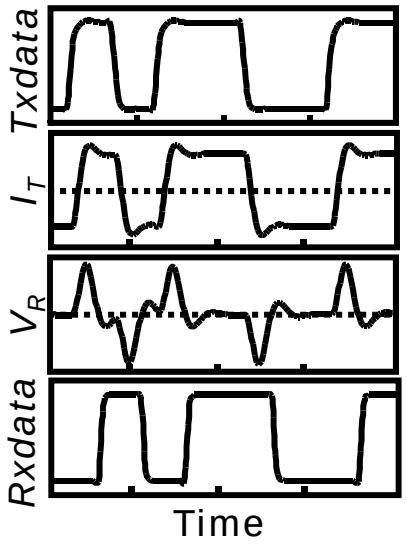


ISSCC2004, pp.142-143



- Inductive coupling
  - data communication through chips
- Transceiver: digital CMOS circuits

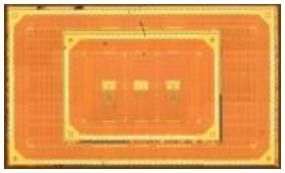




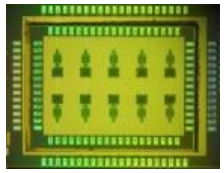
- Coil: multi-layer standard wires
  - Logic interconnections go across coil
  - Coil can be placed anywhere (above SRAM)
- Digital CMOS circuit solution
  - Eventually zero cost

Performance of TCI

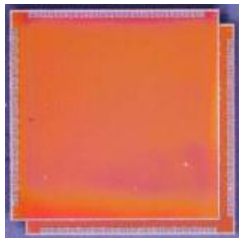
High Speed



11Gb/s/ch
(0.18μm)
ISSCC2008



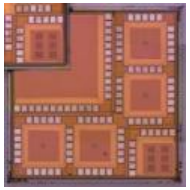
30Gb/s/ch
(65nm)
A-SSCC2010



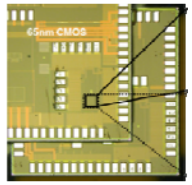
8Tb/s
(1000ch in 2.5mm^2)
ISSCC2010

Aggregated data rate is raised by increasing number of channels.

Low Power



0.14pJ/b
(90nm)
ISSCC2007

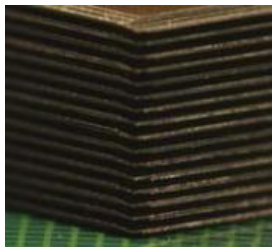


0.01pJ/b
(65nm)
JSSC2011

ESD protection device (>0.5pJ/b) can be eliminated.

High Integration

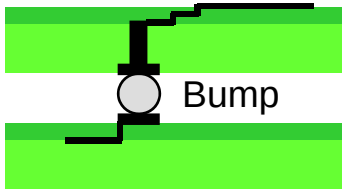
64-die stacking
ISSCC2009



128-die stacking
ISSCC2010

Low Height
Low Thermal Resistance

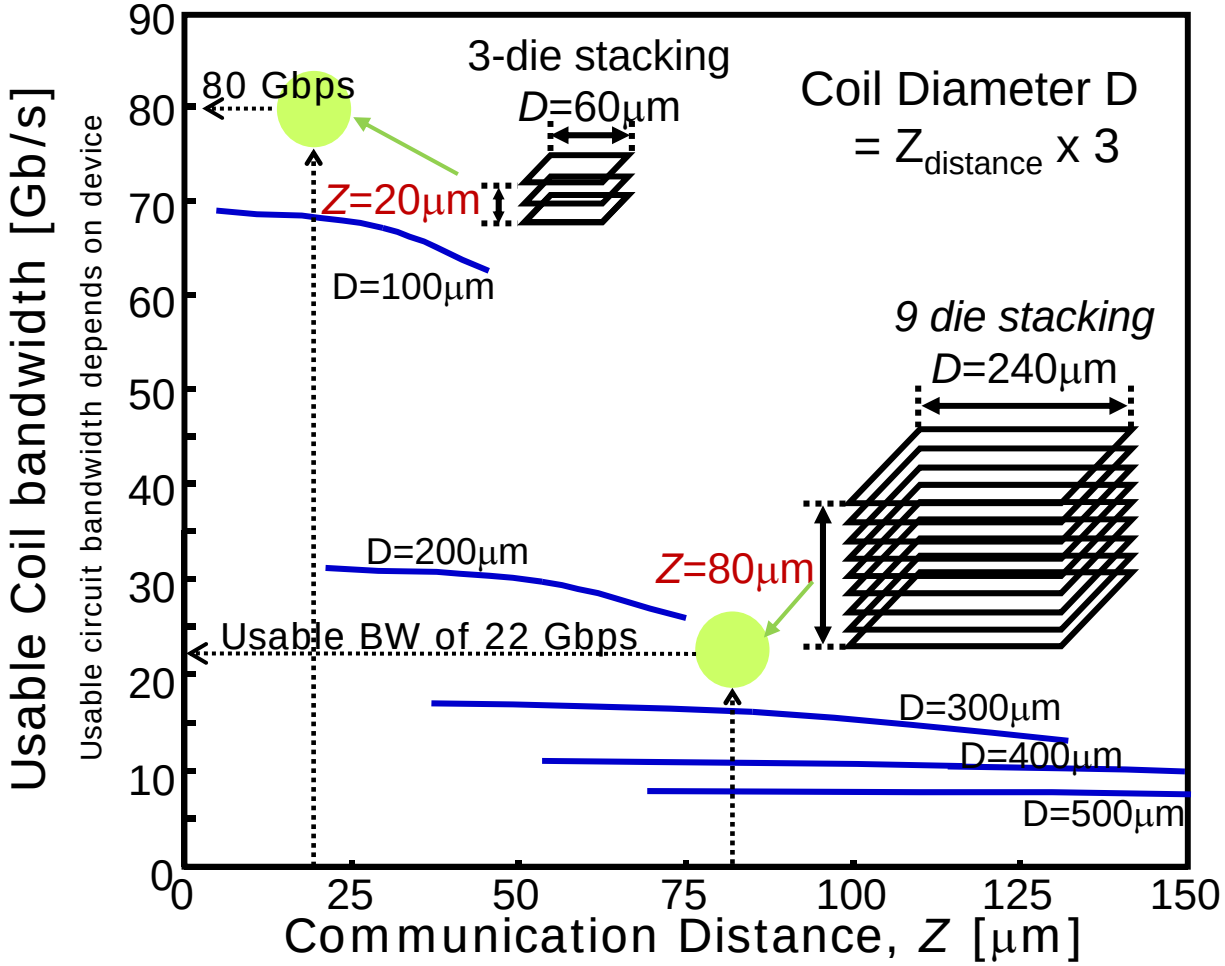
TCI



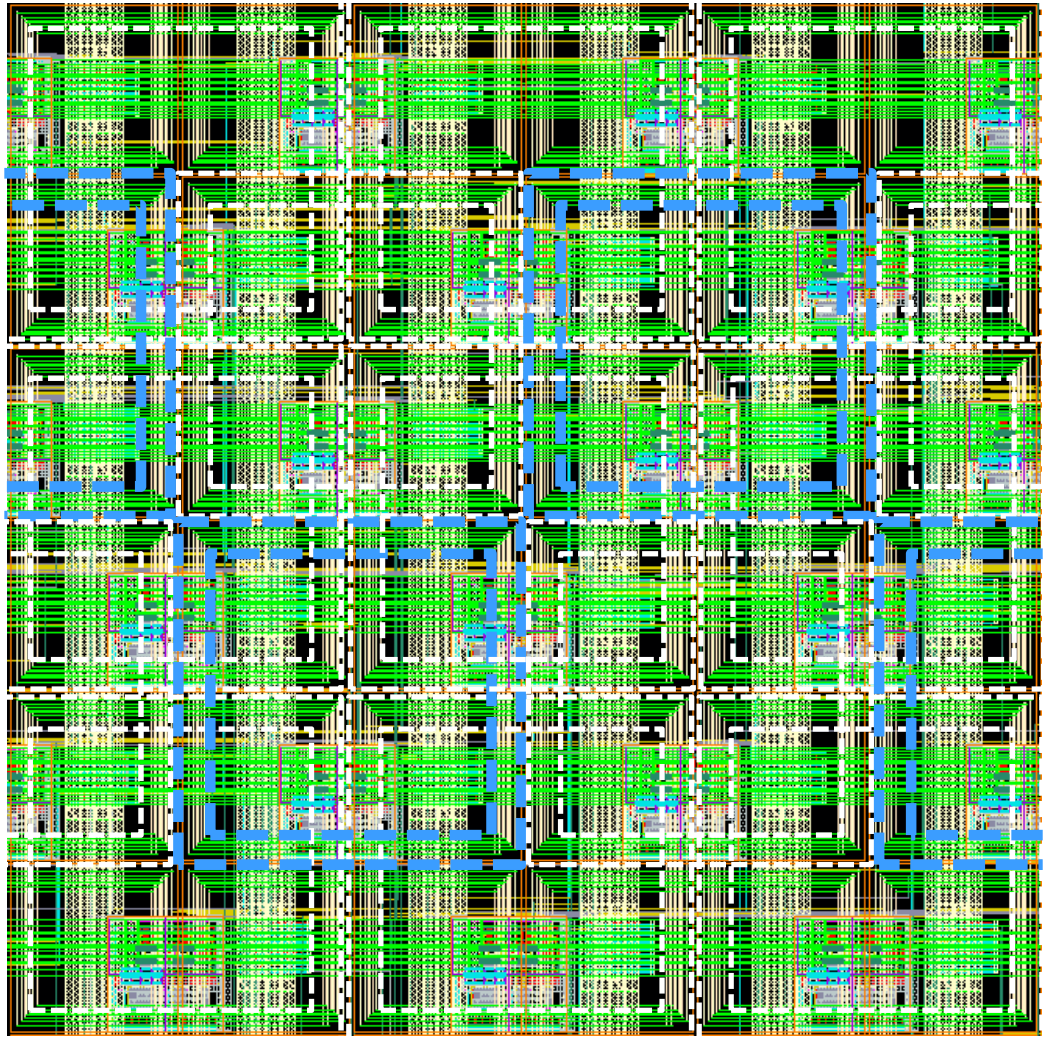
TSV

TCI Coil Design

Data rate goes up dramatically with smaller *Z*

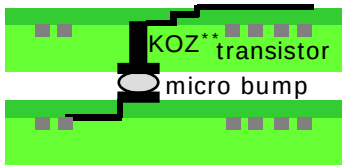
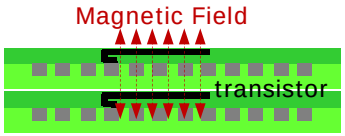


TCI Layout



- Similar to typical CMOS layout
- Coils of 100um size are formed by
  M9 and M10 for TX,
  M7 and M8 for RX,
  with power/signal lines crossing
- Accommodate circuits under the coil
- Coils are overlapped and accessed by PDMA to avoid crosstalk
  - at phase 1
  - at phase 2
  - at phase 3
  - at phase 4

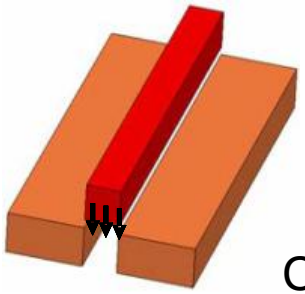
TSV vs. TCI

	TSV	TCI
		
Solution	Mechanical in package	Electrical on wafer
Wafer Technology Package Technology Miniaturization Yield Eco-system	Additional steps needed OSAT* involved Difficult Low, difficult to improve New model needed	Standard CMOS Conventional Easy High (~100%) Conventional model
Additional Cost	> 40%	A few %
Placement	Dedicated area w/KOZ**	Unconstrained
Speed	< 512 GB/s	> 512 GB/s
ESD Protection	Needed	No need
Power Dissipation	High	Low

OSAT*: Outsource Assembly and Test, KOZ**: Keep Out Zone

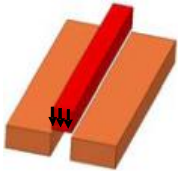
3D Scaling Scenario

- Cost/Performance will be improved by 3D scaling scenario.
- Field Effect Transistor (Moore's Law)



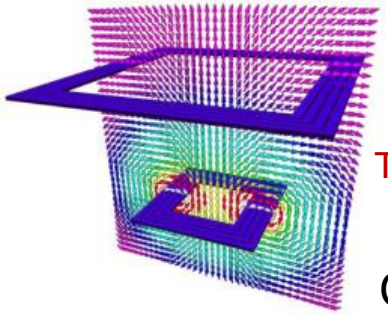
Size:1/2x
Voltage:1/2x

Speed:2x
Power/Area:1x



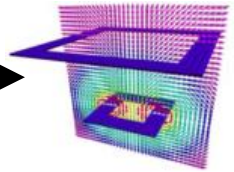
Constant Electric Field Scaling

- Inductive Coupling Link (3D Scaling Law)



Thickness:1/2x

Data Rate/Area:8x
Energy/bit:1/8x



Constant Magnetic Field Scaling

evaluation value	dimension	scaling
Device size	$[x]$	$1/\alpha$
Voltage	$[V]$	$1/\alpha$
Current	$[I]$	$1/\alpha$
Capacitance	$[C]\sim[xx/x]$	$1/\alpha$
Delay time	$[t]\sim[CV/I]$	$1/\alpha$
Chip thickness	$[z]$	$1/\zeta$
Coil size	$[D]$	$1/\zeta$
Coil turn number	$[n]$	$\zeta^{0.8}$
Inductance	$[L]\sim[n^2D^{1.6}]$	1
Magnetic coupling	$[k]\sim[z/D]$	1
Received signal	$[v_R]\sim[kL(I/t)]$	1
Data rate / channel	$[1/t]$	α
Channel / area	$[1/D^2]$	ζ^2
Data rate / area	$[1/tD^2]$	$\alpha\zeta^2$
Energy / bit	$[IVt]$	$1/\alpha^3$

Suppose 8mm-square 4 chips are stacked. When each die is thinned from 50um to 10um, number of on-chip coils are increased from 700 to 17,500, yielding 25x speed improvement.

Performance of TCI in 7nm CMOS

Chip thickness	50 μm	25 μm
Coil size	150 μm	75 μm
Data rate per coil	50 Gb/s/coil	64 Gb/s/coil
Area efficiency	2 Tb/s/mm^2	11 Tb/s/mm^2
Power efficiency	30 fJ/bit	25 fJ/bit
Aggregate data rate when using 8mm x 1mm Si area	18 Tb/s	91 Tb/s
Power dissipation when using 8mm x 1mm Si area	0.5 W	2.2 W

SPICE simulation performed with Predictive Technology Model (http://ptm.asu.edu/)

3-D NoC by TCI

- JSPS project led by Prof. Amano, Prof. Matsutani
  - A Study on Building-Block Computing Systems using TCI
  - Inter-chip wireless inductive coupling techniques, self-organized network-on-chips, fault tolerant architectures, optimized power control, and a flexible operating system with virtualization facilities are investigated
  - http://www.am.ics.keio.ac.jp/kaken_s/

- 3-D NoC with TCI will be presented at IEEE A-SSCC2016
  - Collision detection scheme by sensing magnetic field
  - 44-bit packet transceiver of PER < 10^{-9}

Outline

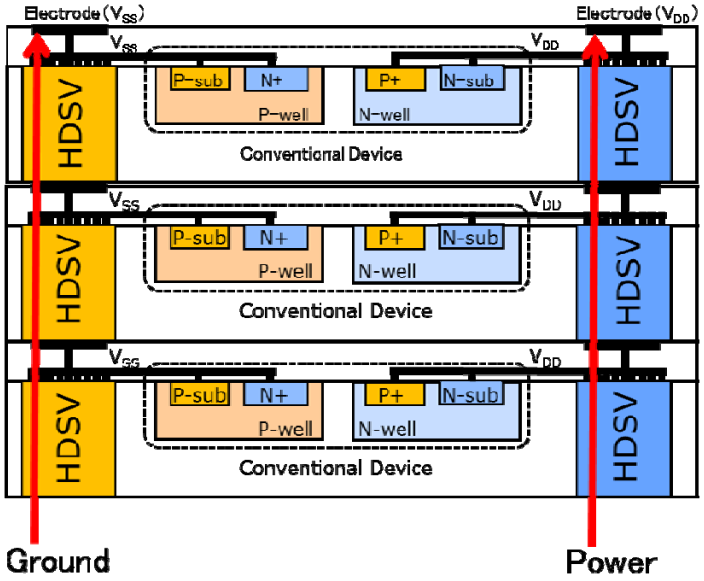
- Near-Field Coupling Integration Technology
- Transmission Line Coupler (TLC)
- ThruChip Interface (TCI)
- Challenges
  - Highly Doped Silicon Vias (HDSV)
  - TCI_2.9D/2.5D/2.0D
- ACCEL
  - 100GFLOPS/W Computer and 512GB/s DRAM

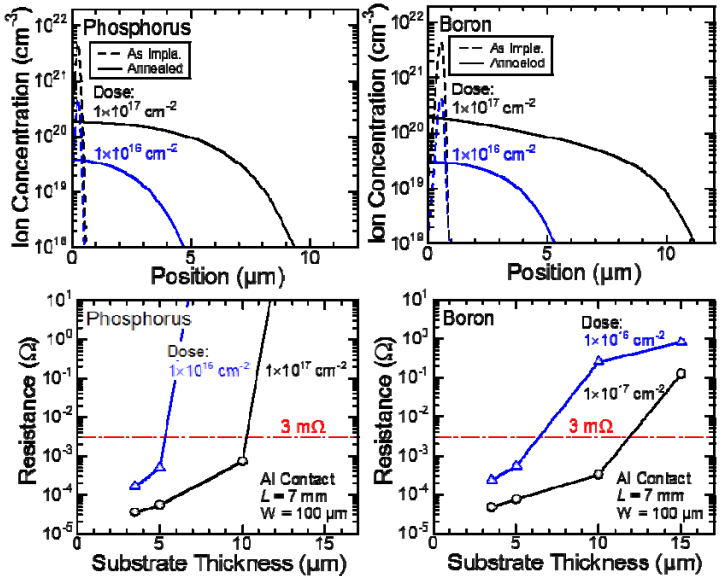
Remaining Challenges

- Proof with DRAM
  - Influence of magnetic field to DRAM
  - Influence of DRAM (plate, cylinder, power mesh) to magnetic field
- Power Supply
  - New way of power delivery to create synergy with TCI is expected.
  - Highly Doped Silicon Vias (HDSV) is proposed.
    Idea is received highly in IEDM but needs proof.
- Heat Removal
  - Heat keeps from die stacking.
  - Inductive coupling for horizontal link (TCI_2.5D/2D) is developed.

Highly Doped Silicon Vias (HDSV)

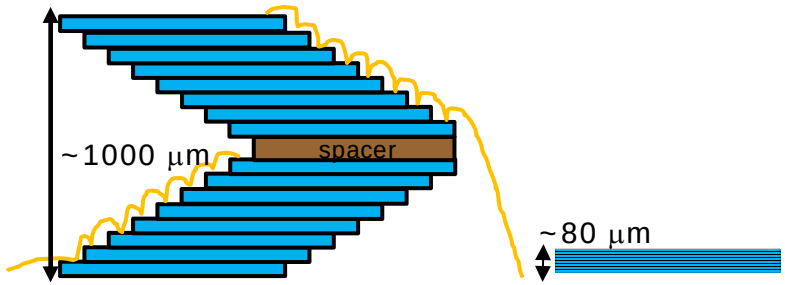
IEDM2014, 18.6.

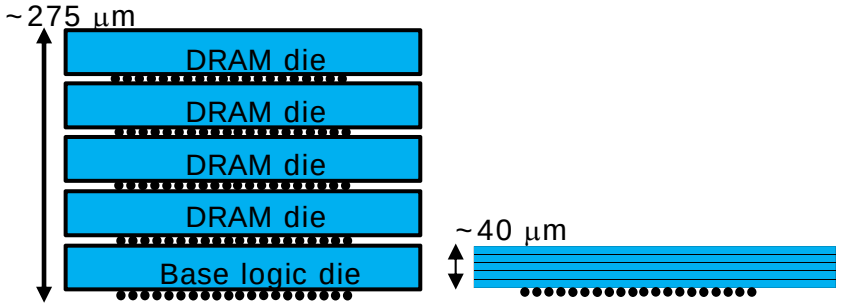




- A deeper and more highly doped well is used to make a low resistance HDSV.
- The HDSV on one die and electrodes on the next die are connected by pressure from a Room-Temperature Wafer Level Bonding machine to create larger stacks.
- TCAD indicates resistance < 3mΩ when substrate <5um, dose: 1x10^{16} cm^{-2}, implant: 200 keV, annealing: 50h, 1050°C.
- 0.7 mm^2 net area is required (can be divided), good only for power delivery.
- Low cost process by implants

Memory Stacking with TCI and HDSV





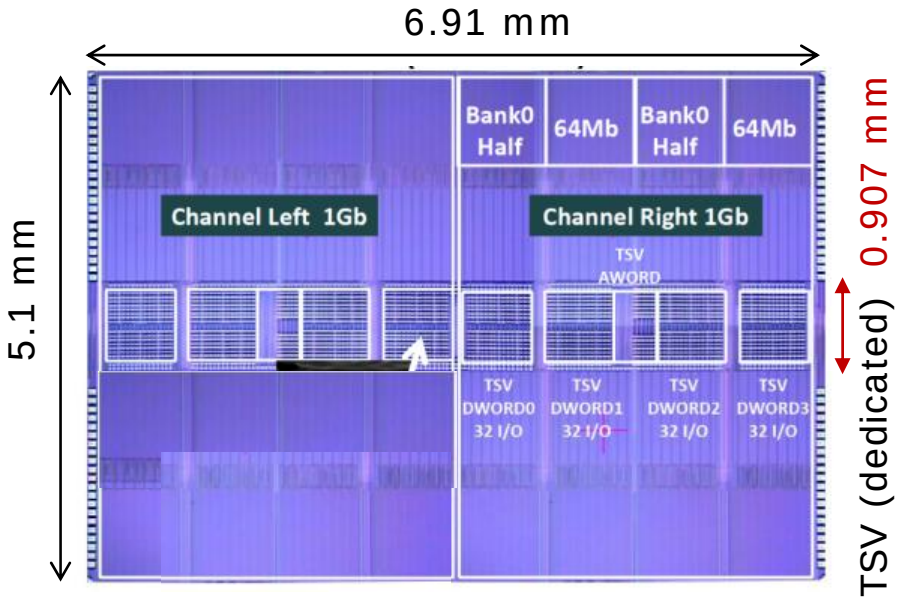
	NAND Stacking		DRAM Stacking	
	wire bond	TCI, HDSV	TSV	TCI, HDSV
# stacked die	16	16	5	5
Die pitch	50μ	5μ	55μ	8μ
Total height	~1000μ	~80μ	~275μ	~40μ
Die area	1x	~0.9x	1x	~0.9x
Data link	wire bond	TCI	TSV	TCI
Power delivery	wire bond	HDSV	TSV	HDSV
IO energy/bit	1x	< 1/400x	1x	< 1/10x
IO data rate/area			~ 200 Gb/s/mm^2	~ 860 Gb/s/mm^2

Hot Chips 2014

128GB/s HBM Case Study

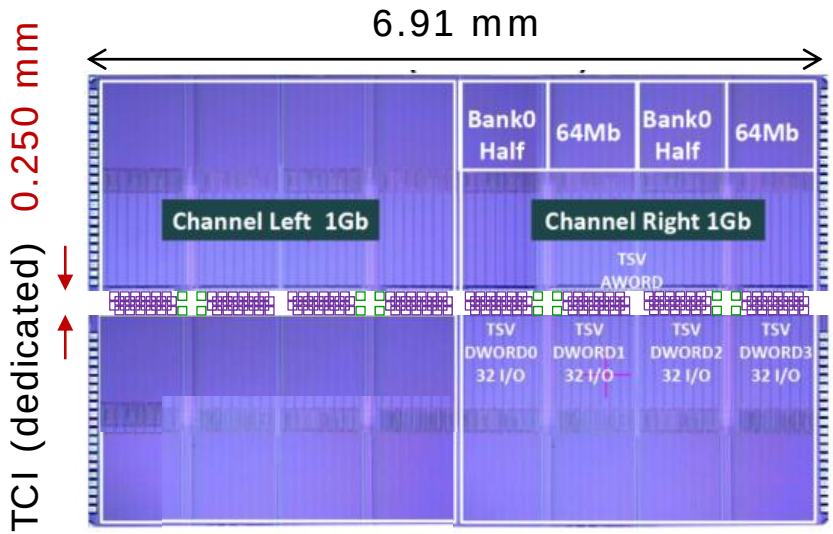
- TCI reduced chip size by 13% than TSV.

TSV

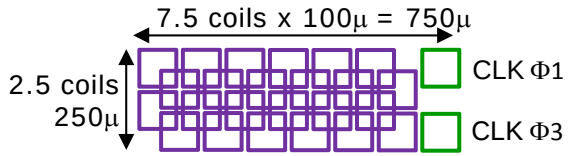


SK Hynix, ISSCC2014
1Gb/s/TSV*1024 TSV=128 GB/s

TCI, HDSV



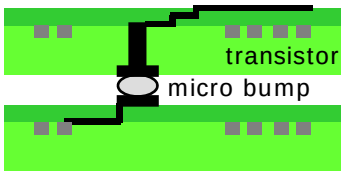
Suppose chip thickness of 10um, stacking of 5 chips.
Communication distance is 40um, coil diameter is 100um.
8 Gb/s/coil*16 coil *8 = 128GB/s



Hot Chips 2014

TCI Can Use Whole Chip Area

TSV
need to be placed
away from active area



Area +18%

Area +36%

1024 TSV

2048 TSV

Impractical for further addition of dedicated area for TSV

Memory Area

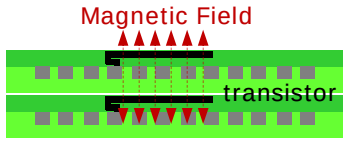
I/O Area

128GB/s

256GB/s

512GB/s ...

TCI
can be placed in active area



Area +3%

Area +6%

With addition of one metal layer, TCI can be placed in memory area (need proof)

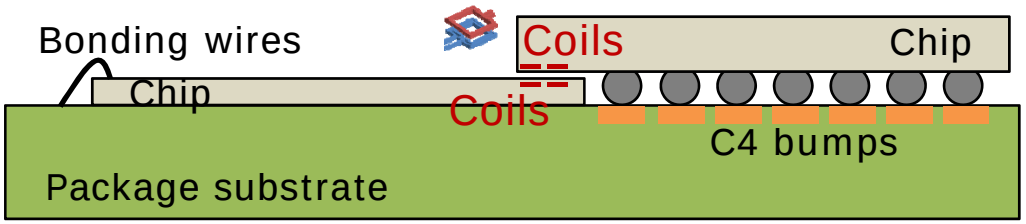
208 coil

416 coil

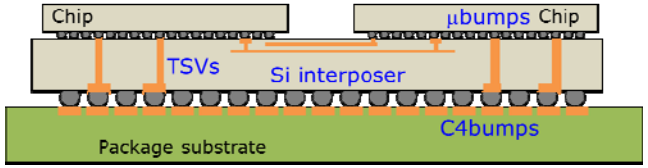
5096 coil

...

TCI_2.9D, 2.5D, 2.0D for Heat Removal

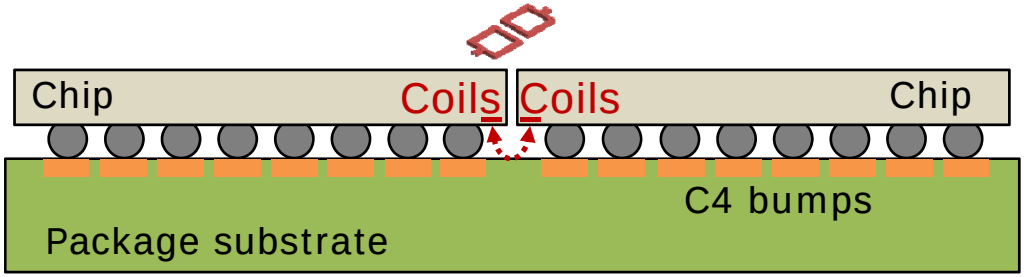


(a) TCI_2.9D packaging.



Conventional 2.5D packaging by Si interposer with μbumps and TSVs.

(b) TCI_2.5D packaging with small Si interposer.



(c) TCI_2.0D packaging.

TCI can release mechanical constraints such as stress

Outline

- Near-Field Coupling Integration Technology
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- ThruChip Interface (TCI)
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  - Highly Doped Silicon Vias (HDSV)
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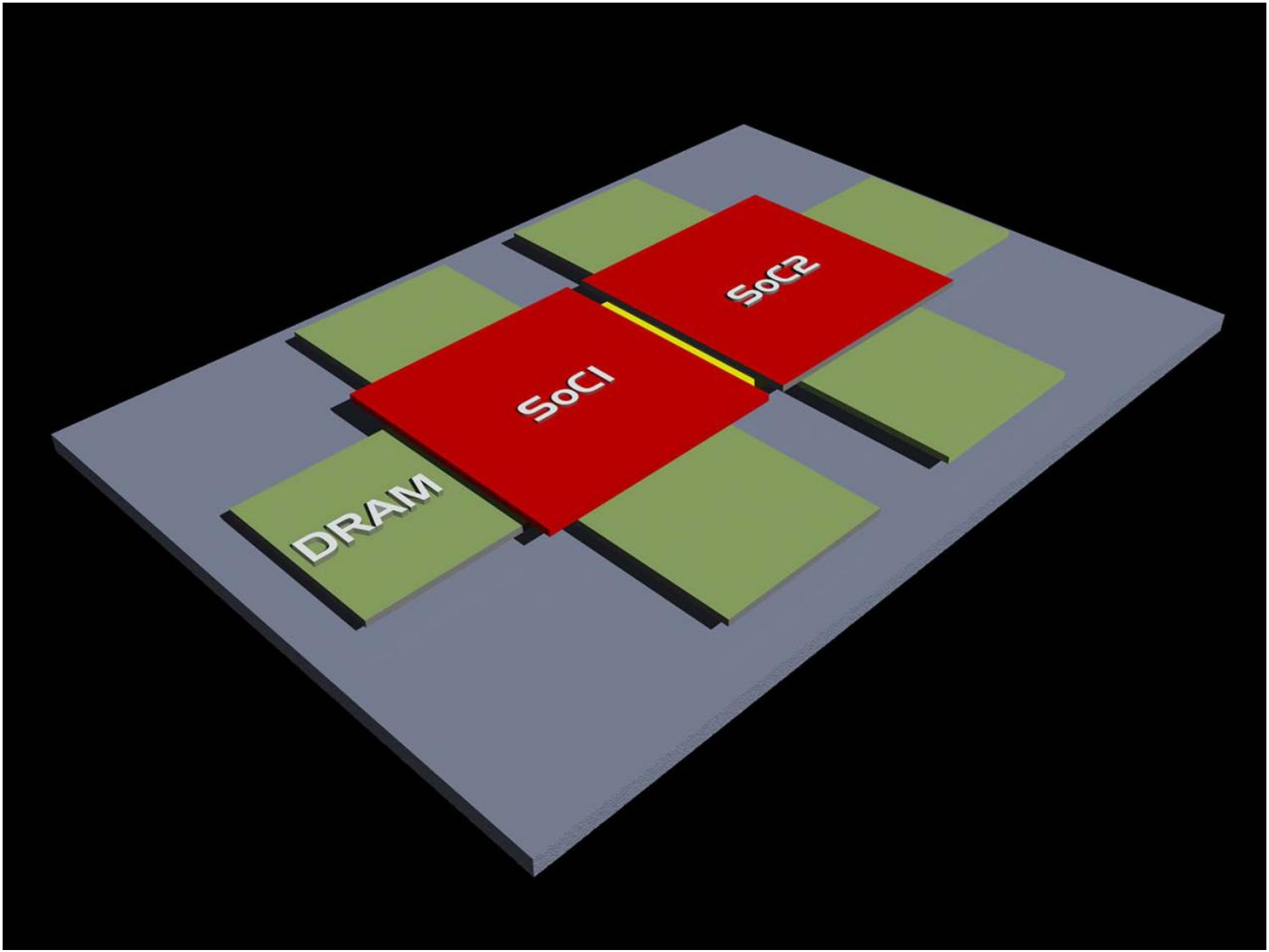
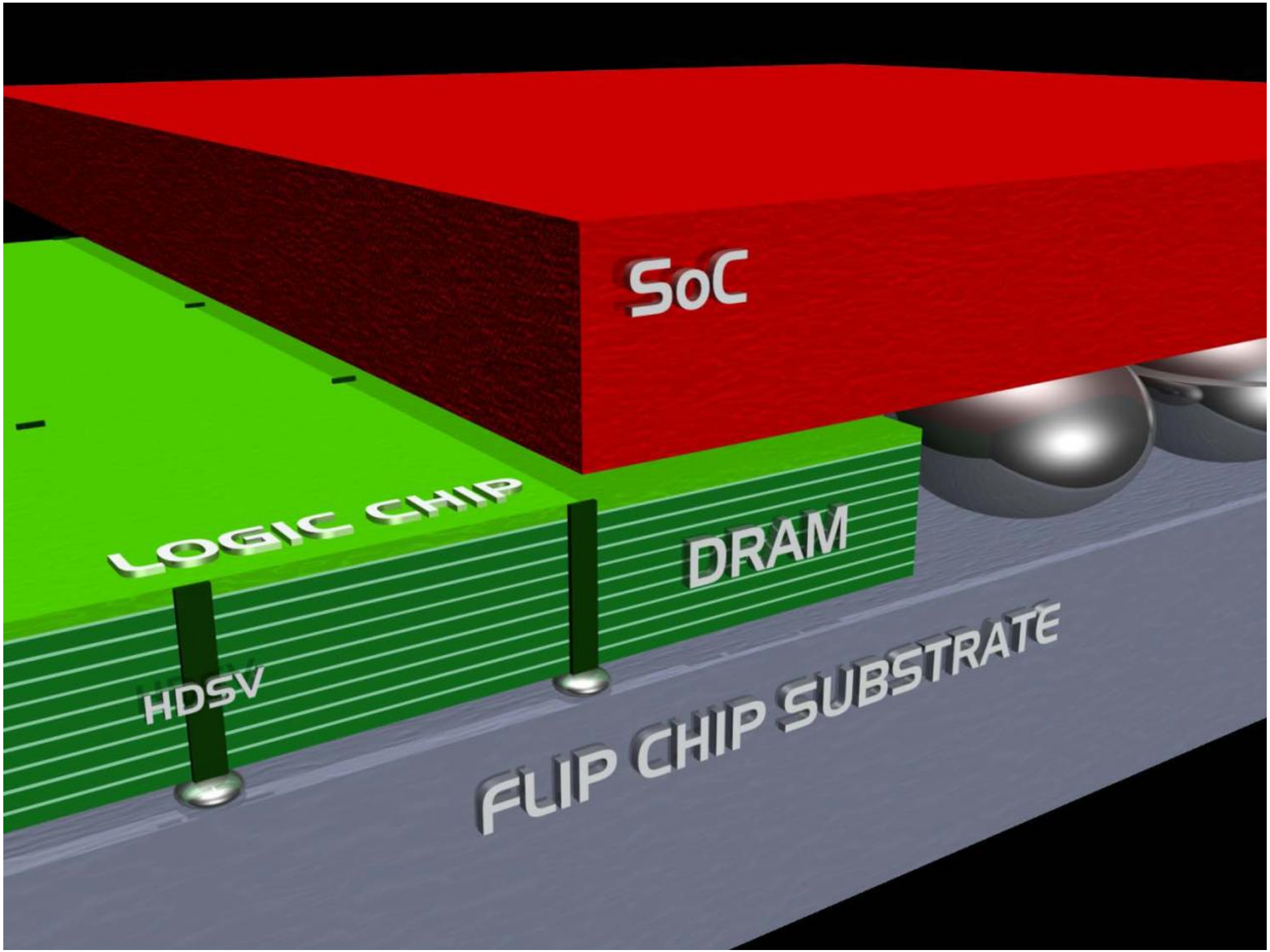
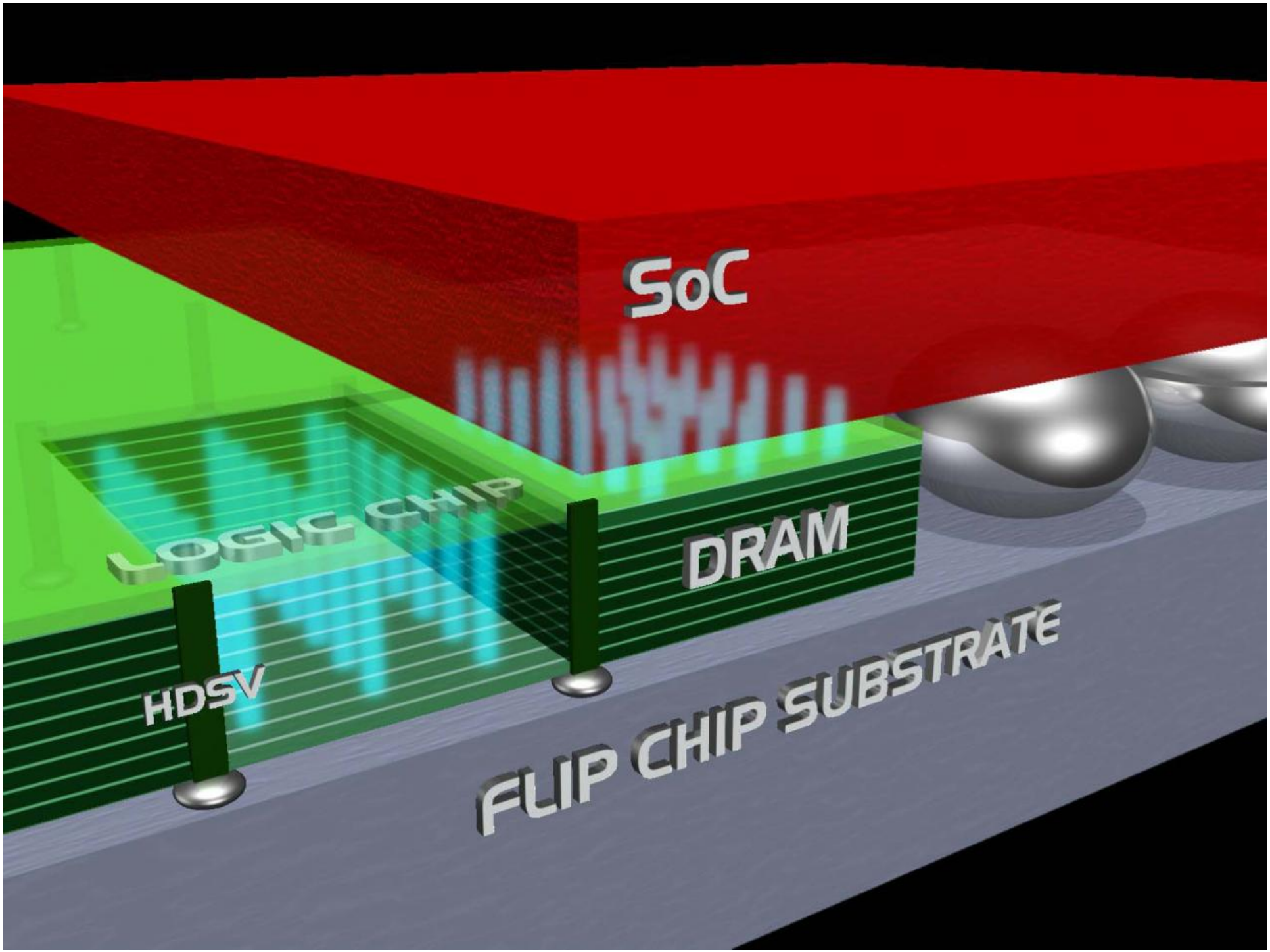
- ACCEL
  - 100GFLOPS/W Computer and 512GB/s DRAM

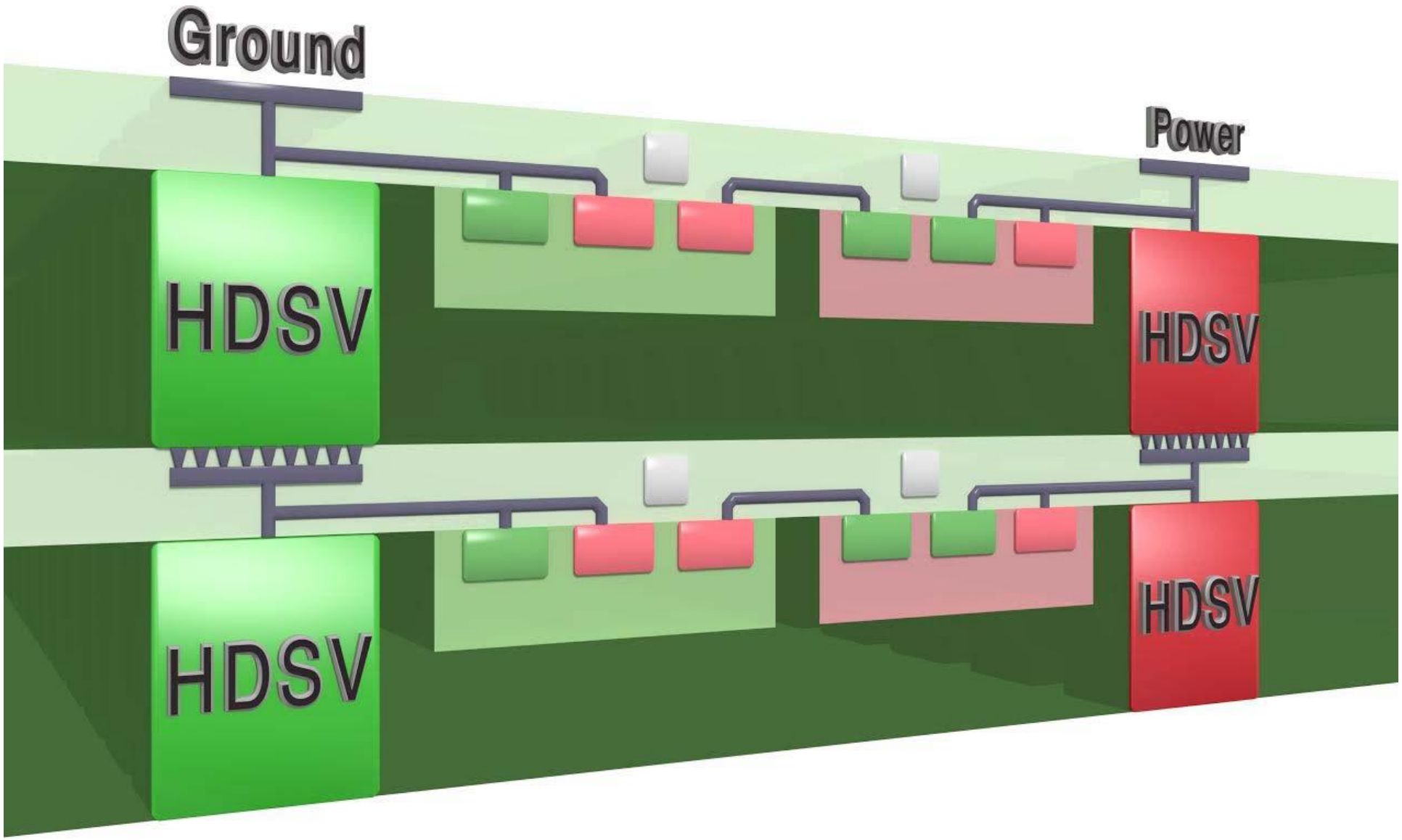
JST ACCEL Project (2015-2019)

- Goal
  - Mobile supercomputer with world's best power efficiency of 100GFLOPS/W (2019)
- Milestone
  - 512GB/s 8GB 8-Stacked DRAM (2017)
- Technology
  - 3D Integration using Near-Field Coupling Integration Technology
- Further Challenges
  - AI computer equipped with both a left brain and a right brain to explore a new paradigm of information processing
  - Left brain employing stored program system by 3D Integration
  - Right brain employing virtual hard-wired logic system by 4D Integration (3D + DRP with DNN and DL; not mentioned today)


SoC2
SoC1
DRAM

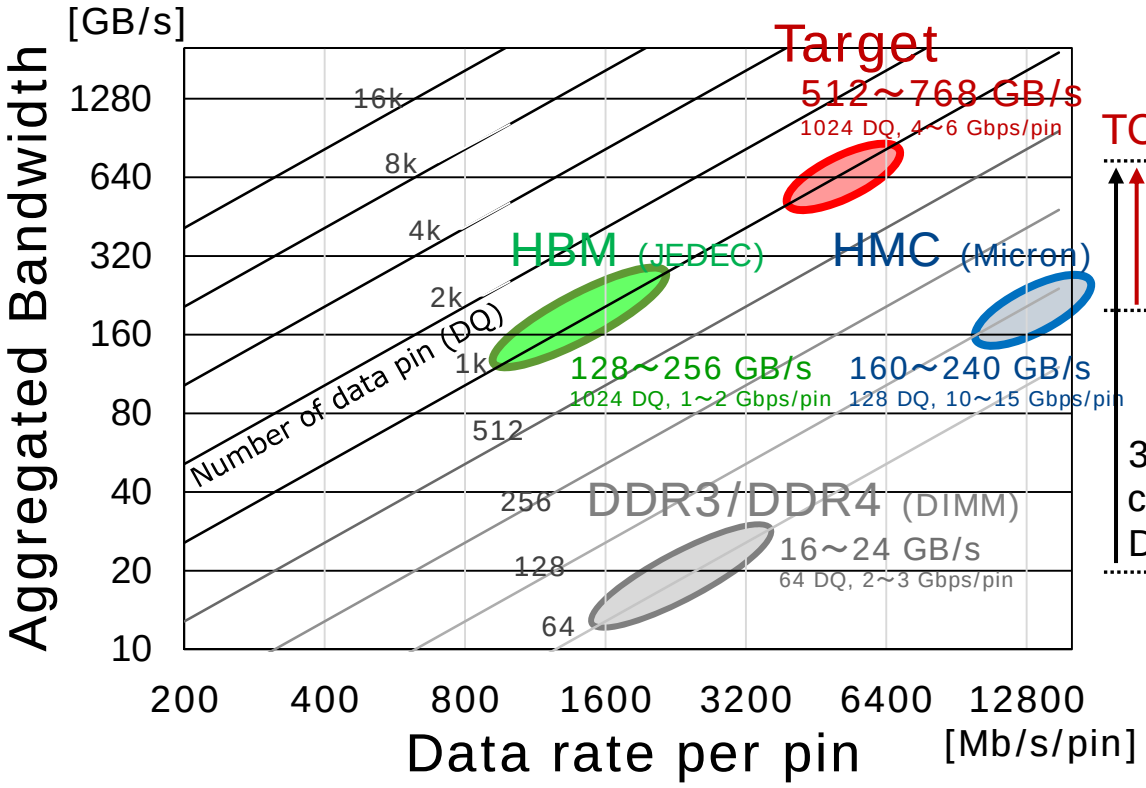

SoC
LOGIC CHIP
DRAM
HDSV
FLIP CHIP SUBSTRATE

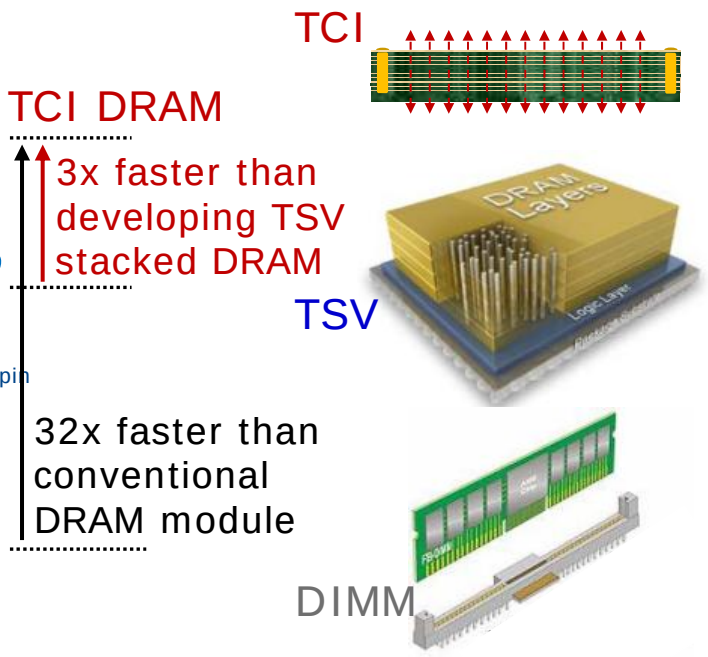

SoC
LOGIC CHIP
DRAM
HDSV
FLIP CHIP SUBSTRATE


Ground
Power
HDSV
HDSV
HDSV
HDSV

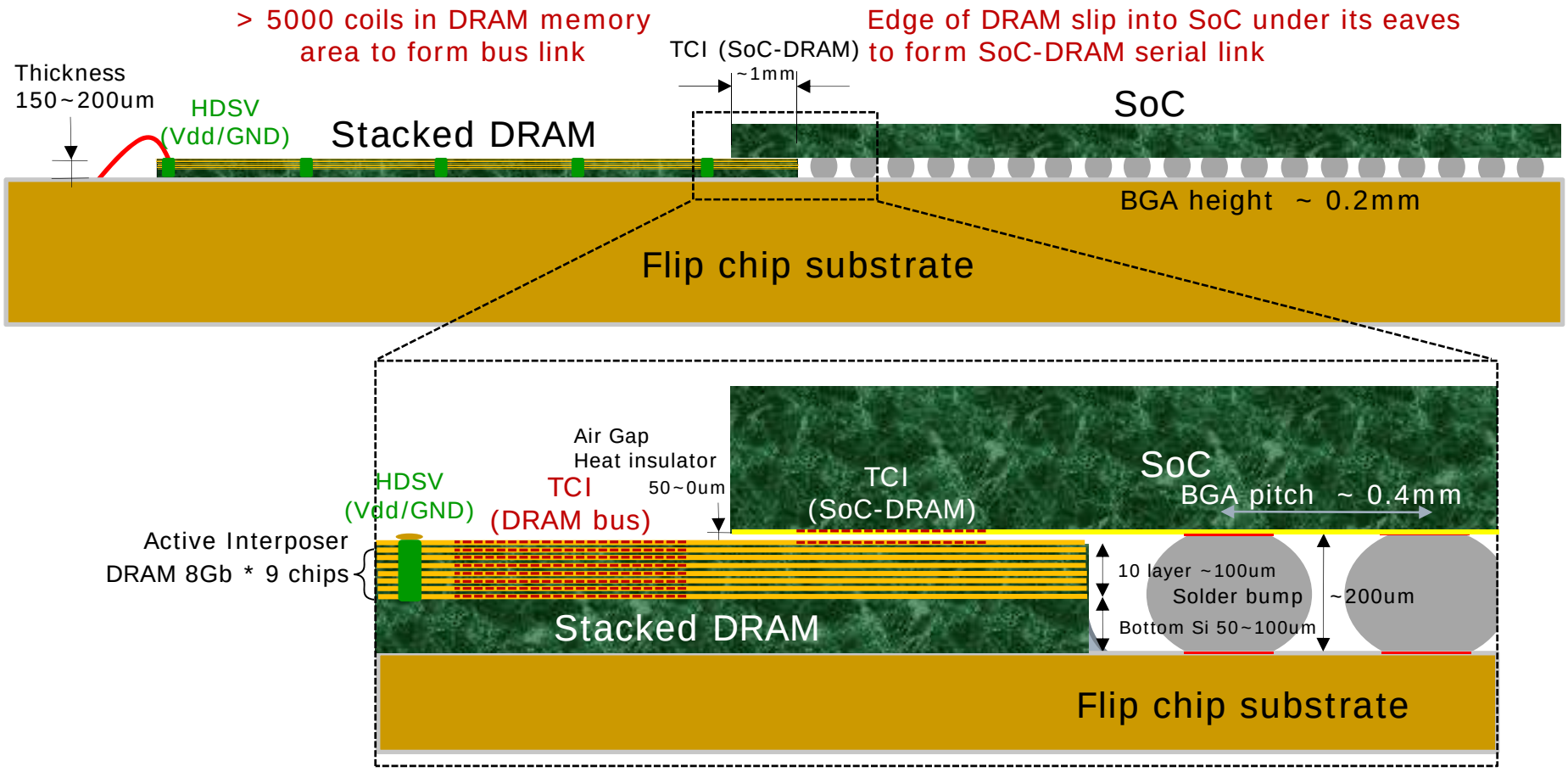
512GB/s 8GB TCI DRAM

- Target of TCI DRAM is 3x faster than HBM and HMC.





100GFLOPS/W Computer



Summary

- Near-Field Coupling Integration Technology challenges to “Tyranny of Numbers” in post-Moore.
- Transmission Line Coupler (TLC) using electromagnetic coupling enables contactless connector for modular design.
- ThruChip Interface (TCI) using inductive coupling enables die stacking for 3D integration.
- Challenges
  - Proof with DRAM
  - Highly Doped Silicon Vias (HDSV) for power supply
  - TCI_2.9D/2.5D/2.0D for heat removal
- ACCEL aims for 512GB/s DRAM (in 2017) and 100GFLOPS/W computer (in 2019).

Questions

Key References

TCI

[01] *ISSCC 2004*, pp.142-143.
[02] *Symp. VLSI Circuits 2004*, pp. 246-249.
[03] *CICC 2004*, pp.99-102.
[04] *ISSCC 2005*, pp.264-265.
[05] *ISSCC 2006*, pp.424-425.
[06] *ESSCIRC 2006*, pp.3-6.
[07] *ISSCC 2007*, pp.264-265.
[08] *A-SSCC 2007*, pp.131-134.
[09] *ISSCC 2008*, pp.298-299.
[10] *ISSCC 2009*, pp.244-245.
[11] *ISSCC 2009*, pp.480-481.
[12] *Symp. on VLSI Circuits 2009*, pp. 256-257.
[13] *Symp. on VLSI Circuits 2009*, pp. 94-95.
[14] *Symp. on VLSI Circuits 2009*, pp. 92-93.
[15] *CICC 2009*, pp. 449-452.
[16] *A-SSCC 2009*, pp.305-308.
[17] *A-SSCC 2009*, pp.301-304.
[18] *ISSCC 2010*, pp.436-437.
[19] *ISSCC 2010*, pp.440-441.
[20] *ISSCC 2010*, ES3.
[21] *Symp. on VLSI Circuits 2010*, pp. 201-202.
[22] *A-SSCC 2010*, pp.81-84.
[23] *IEDM 2010*, p.17.1.1.
[24] *ISSCC 2011*, pp.490-491.
[25] *ISSCC 2013*, pp. 258-259.
[26] *Hot Chips 2014*.

TLC

[01] *ISSCC 2007*, pp.266-267.
[02] *CICC 2007*, pp.13-2007.
[03] *A-SSCC 2008*, pp.113-116.
[04] *ISSCC 2009*, pp.470-472.
[05] *Symp. on VLSI Circuits 2009*, pp. 26-27.
[06] *ISSCC 2010*, pp.264-265.
[07] *ISSCC 2011*, pp. 492-493.
[08] *A-SSCC 2011*, pp. 145-148.
[09] *ISSCC 2012*, pp. 52-53.
[10] *CICC 2012*, pp. 7.9.1-7.9.4.
[11] *ISSCC 2013*, pp. 214-215.
[12] *ISSCC 2013*, pp. 200-201.
[13] *ISSCC 2014*, pp. 496-497.
[14] *ISSCC 2015*, pp. 176-177.
[15] *ISSCC 2015*, pp. 434-435.
[16] *Symp. on VLSI Circuits 2015*, pp. C128-129.