

#### NoCs: Past, Present and Future

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and Brian Towles tems Laboratory

### NoCs: Connecting people

SPIN: a Scalable, Packet Switched, On-chip Micro-network

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SOC DESIGNS

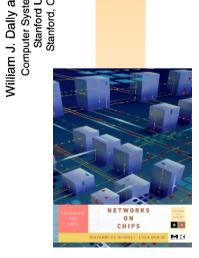
Networks on Chips: A New SoC

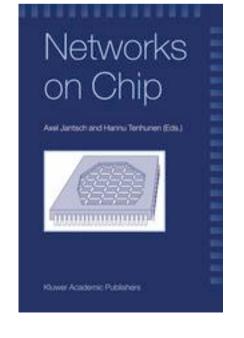
Paradigm



Æthereal Network on Chip: Concepts, Architectures, and Implementations

Kees Goossens, John Dielissen, and Andrei Rădulescu Philips Research Laboratories

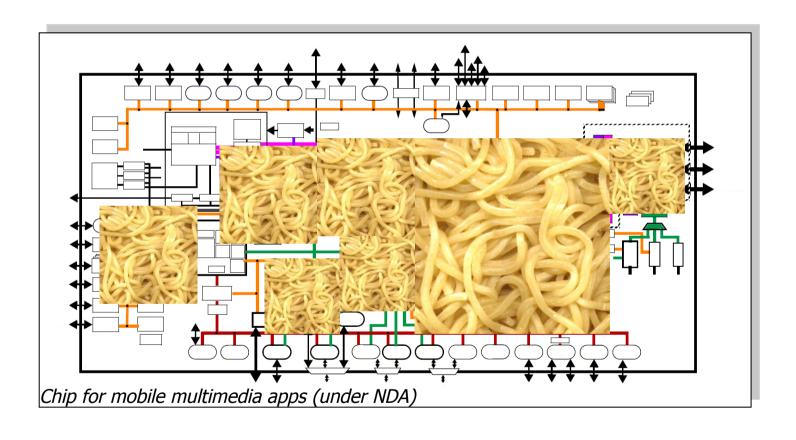




### NoCs: Connecting design

- Connecting scientific communities
  - Multiprocessor Design, Communication, EDA
- Connecting technologies
  - Silicon, optical, RF
- Providing hardware scalability through raising design abstraction level

### The Rise of Networks-on-Chip

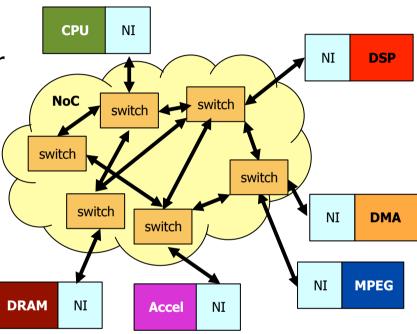




#### The Network-on-Chip Paradigm

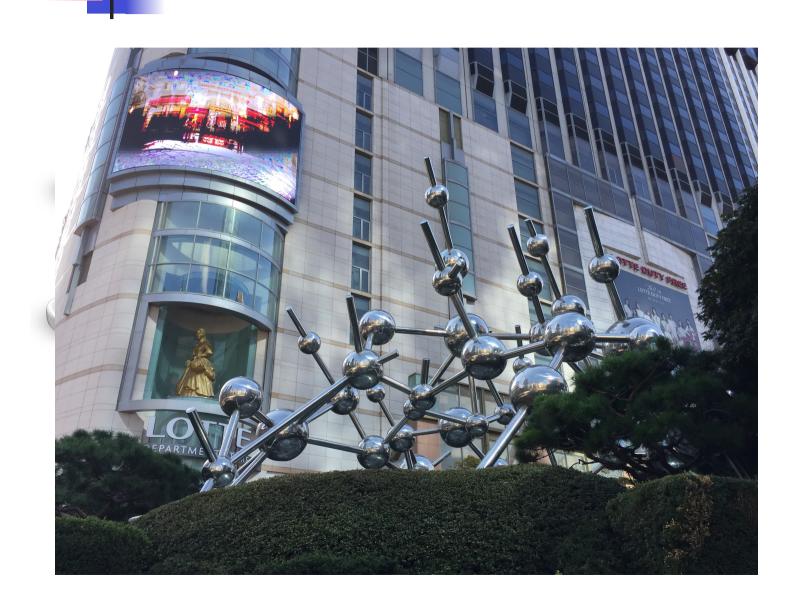
#### The "power of NoCs":

- Clean separation at session layer
  - Cores issue end-to-end transactions
  - Network deals with transport, network, link, physical
- Modularity at HW level: only 2 building blocks
  - Network interface
  - Switch (router)
- Physical design aware (floorplan global routing)

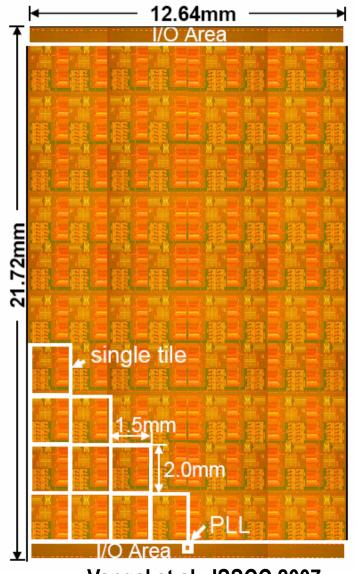


Scalability is supported from the ground up!

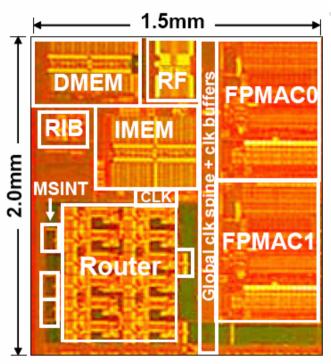
#### NoCs: Past and Present



### **Enabling multiprocessing**

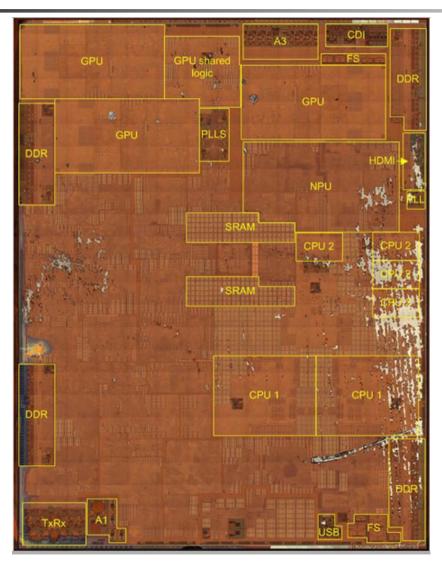


Vangal et al. ISSCC 2007



Technology	65nm CMOS Process
Interconnect	1 poly, 8 metal (Cu)
Transistors	100 Million
Die Area	275 mm <sup>2</sup>
Tile Area	3 mm <sup>2</sup>
Package	1248 pin LGA, 14 layers, 343 signal pins

## **Enabling multiprocessing**

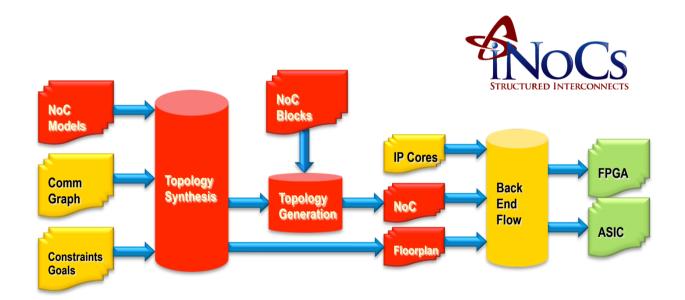


Technology	10nm CMOS Process TSMC
Processor	ARM v8A 6-core
Transistors	4.3 Billion
Die Area	88 mm <sup>2</sup>
Application	mobile
Package	Package on Package With 2GB of memory

Apple A11 SoC

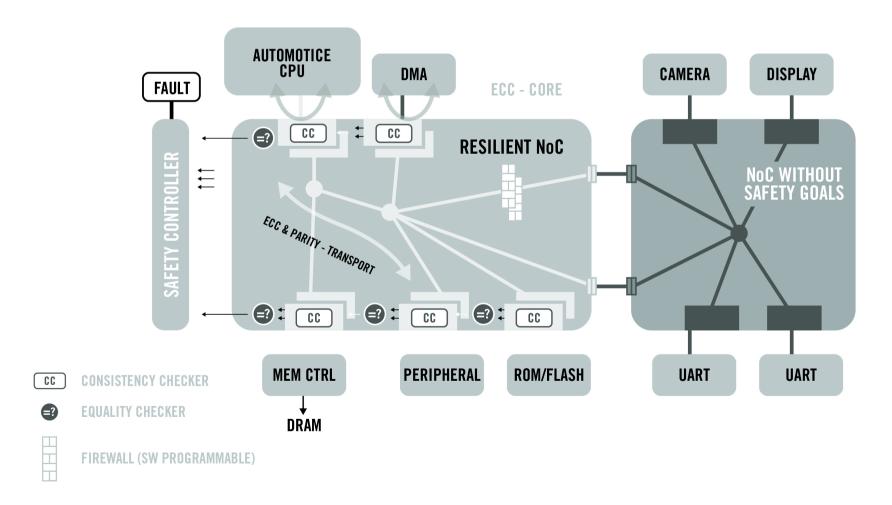
### NoCs: Enabled by EDA

From academic startups



#### NoCs: Enabled by EDA

■ To market leaders: Arteris



#### The Future

Almost all telephones and cars have a NoC





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