Keio University

1858

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Wireless NoC as Interconnection Backbone for Multicore Chips: Promises, Challenges, and Recent Developments

Part IV: 3D WiNoC Architectures

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Keio University, Japan

Outline: 3D WiNoC Architectures

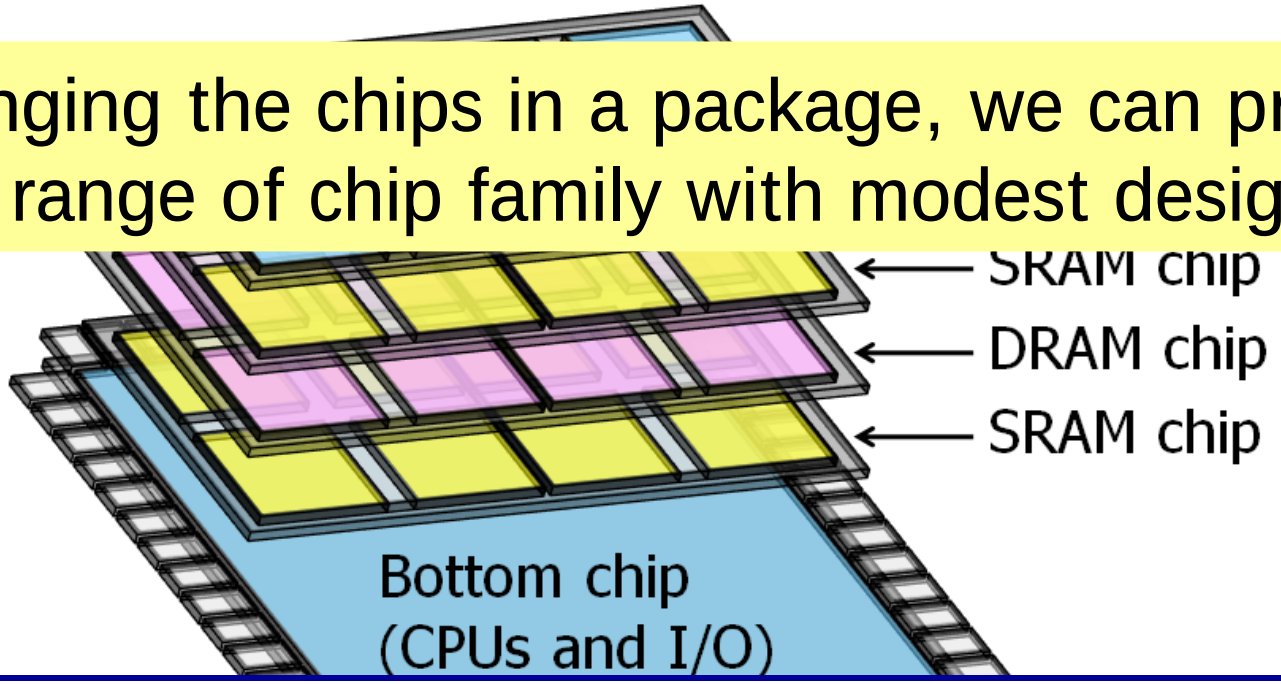
So far we focused on 2D WiNoC architecture and its physical link design. This part explores 3D WiNoC architectures, especially inductive-coupling 3D option.

- 3D IC technologies: Wired vs. Wireless [5min]
- Prototype systems: Cube-0 & Cube-1 [15min]
- Wireless 3D NoC architectures [15min]
  - Ring-based 3D WiNoC
  - Irregular 3D WiNoC
- Experiment results and Summary [10min]

Design cost of LSI is increasing

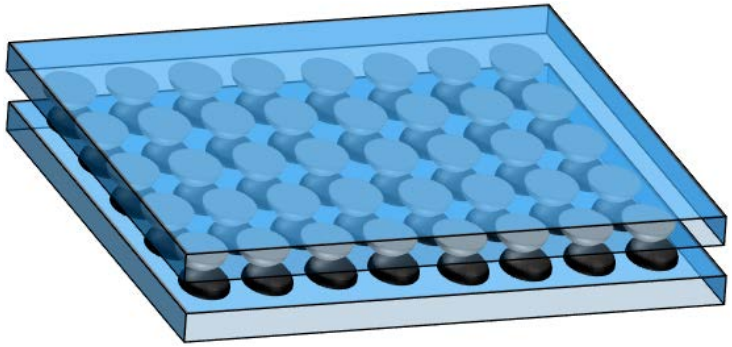
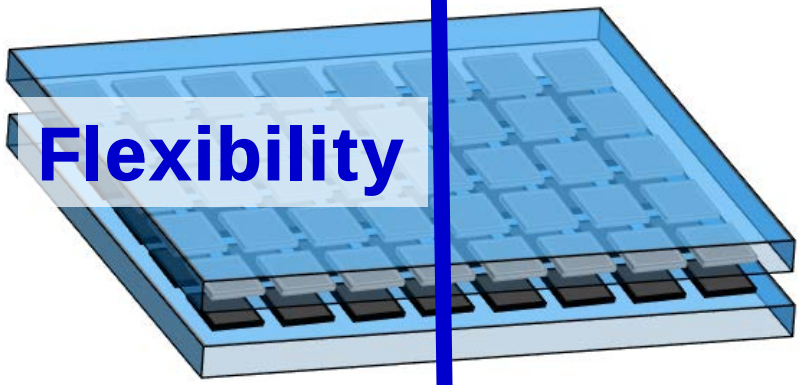
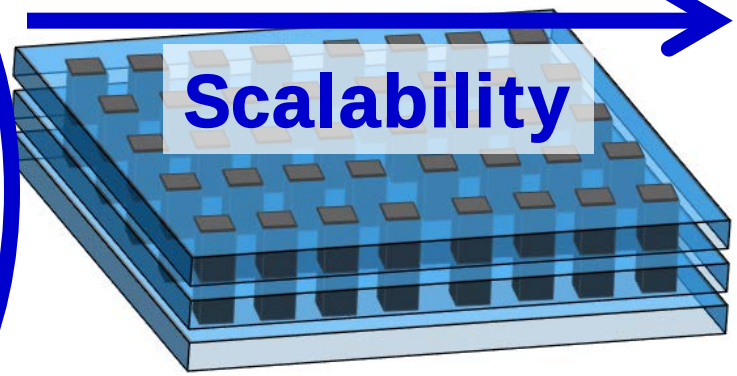
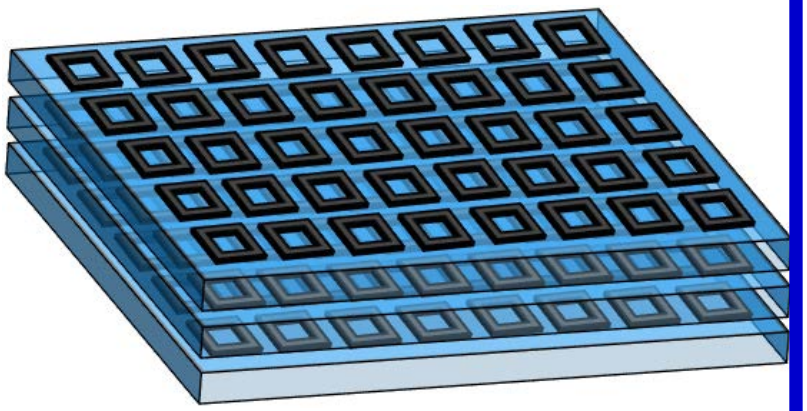
- System-on-Chip (SoC)
  - Required components are integrated on a single chip
  - Different LSI must be developed for each application
- System-in-Package (SiP) or 3D IC
  - Required components are stacked for each application

By changing the chips in a package, we can provide a wider range of chip family with modest design cost



Next slides show techniques for stacking multiple chips

3D IC technology for going vertical

	Wired	Wireless
Two chips (face-to-face)	 Microbump	 Capacitive coupling
More than three chips	 Through silicon via	 Inductive coupling

Flexibility

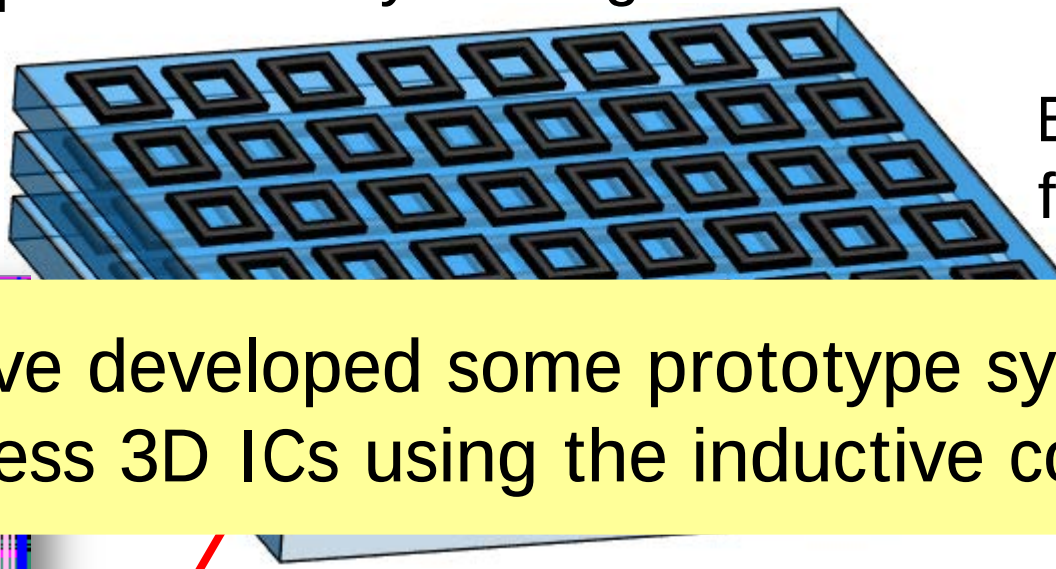
Scalability

Inductive coupling link for 3D ICs

Stacking after chip fabrication

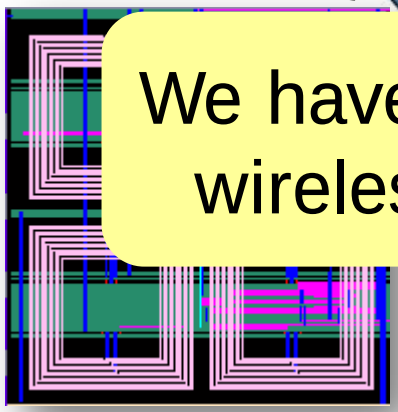
Only know-good-dies selected

More than 3 chips



Bonding wires for power supply

We have developed some prototype systems of wireless 3D ICs using the inductive coupling



Inductor for transceiver

Implemented as a square coil with metal in common CMOS

Footprint of inductor

Not a serious problem. Only metal layers are occupied

Note: This part focuses on inter-chip wireless, not the intra-chip wireless introduced in Parts II and III.

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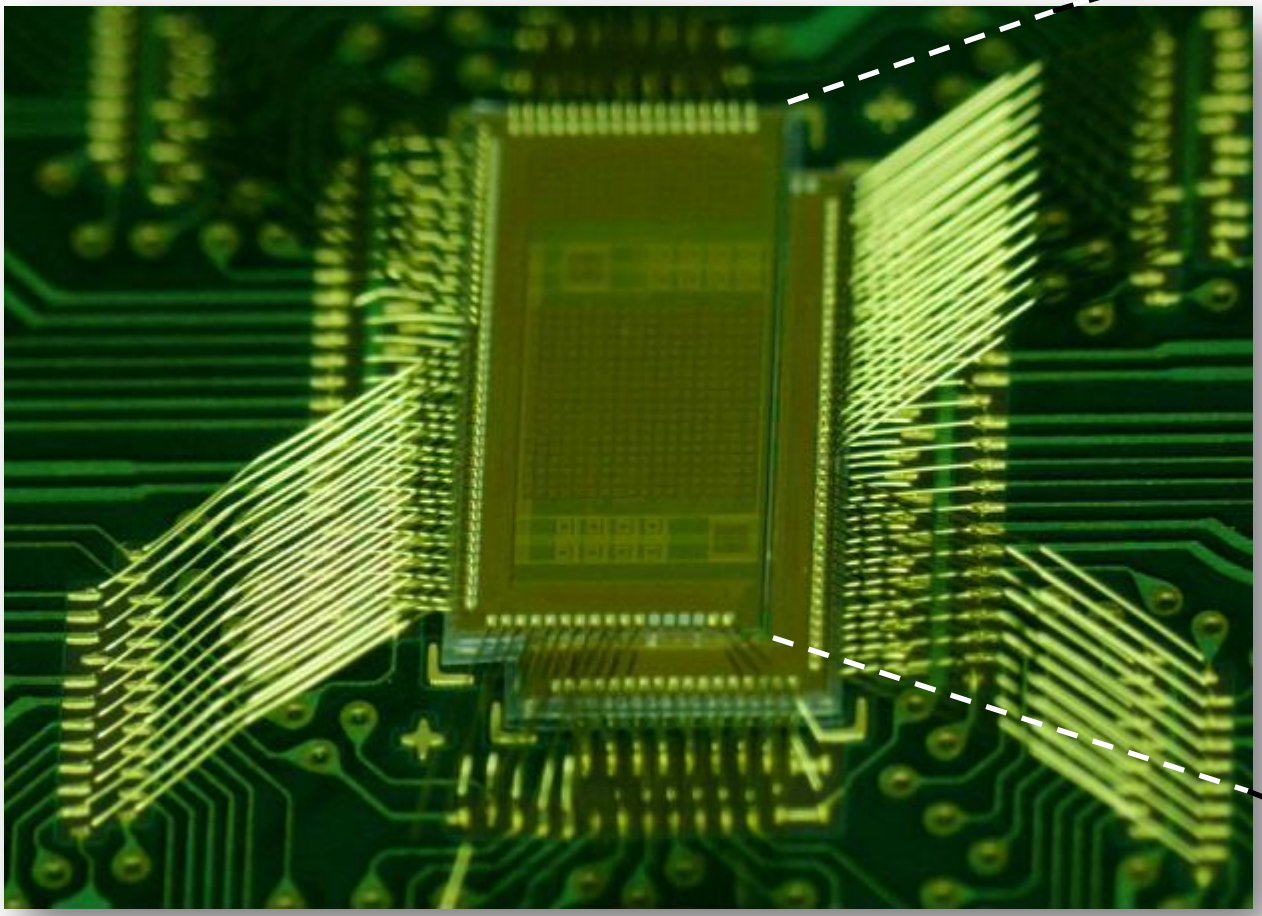
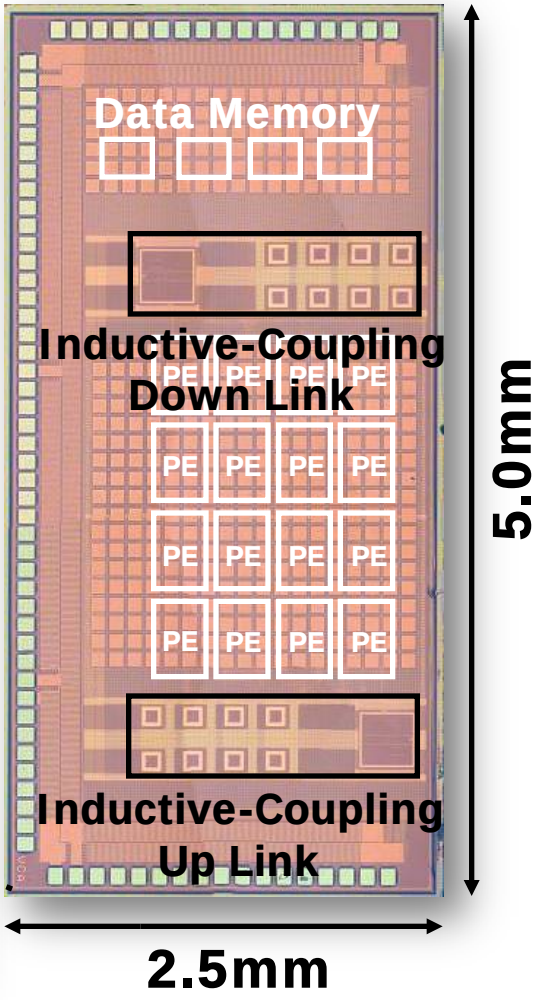
An example: MuCCRA-Cube (2008)

- 4 MuCCRA chips are stacked on a PCB board





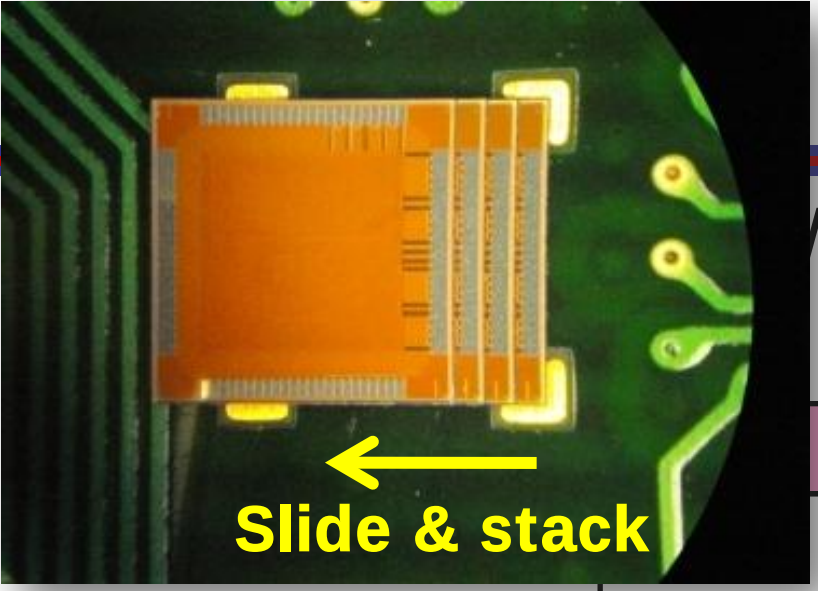
Technology: 90nm

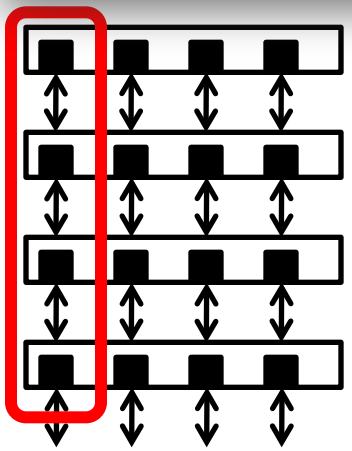
Chip thickness: 85um, Glue: 10um

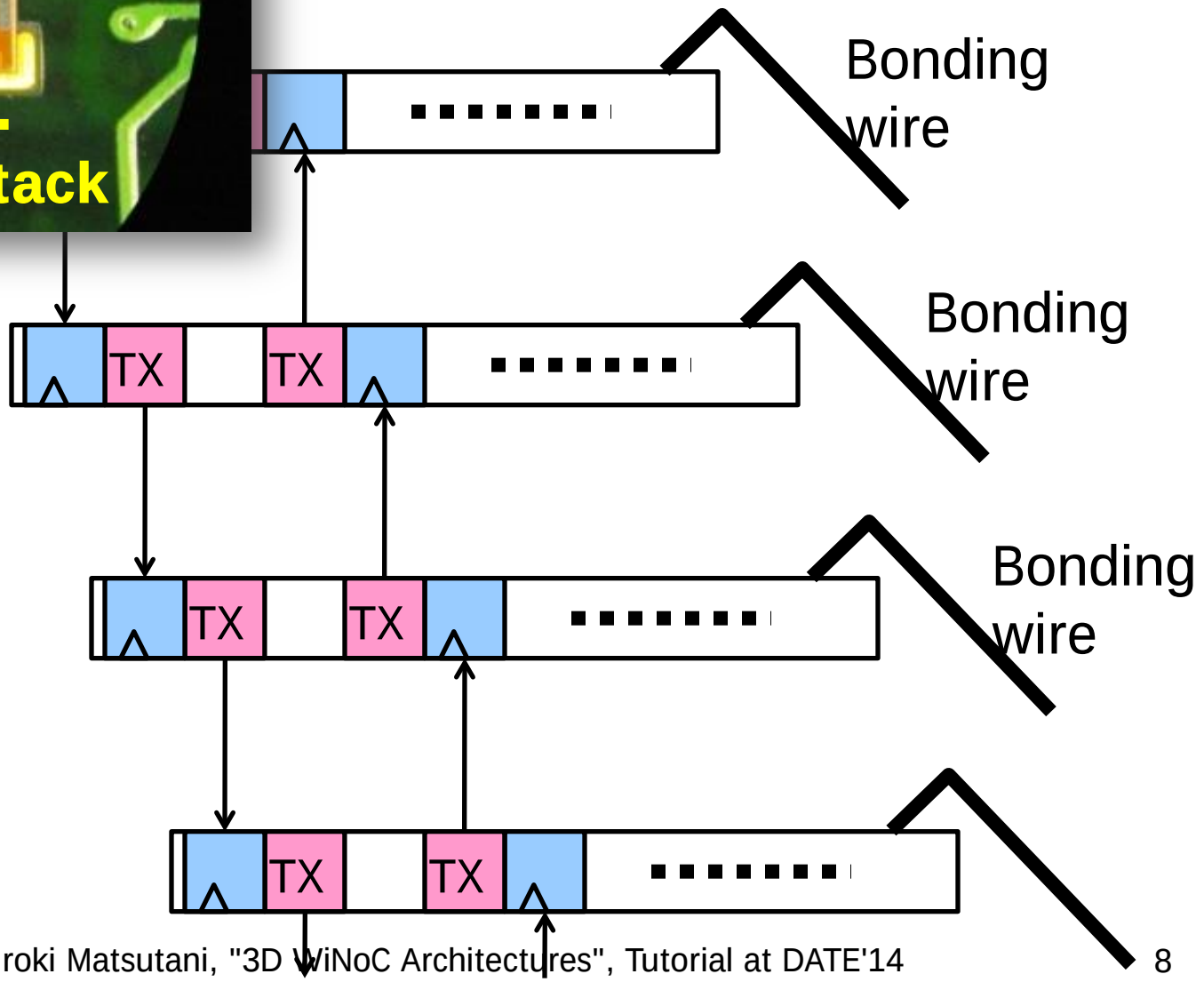
[Saito,FPL'09]

hod: Staircase stacking

/Idle modes (mode change 1-cycle)







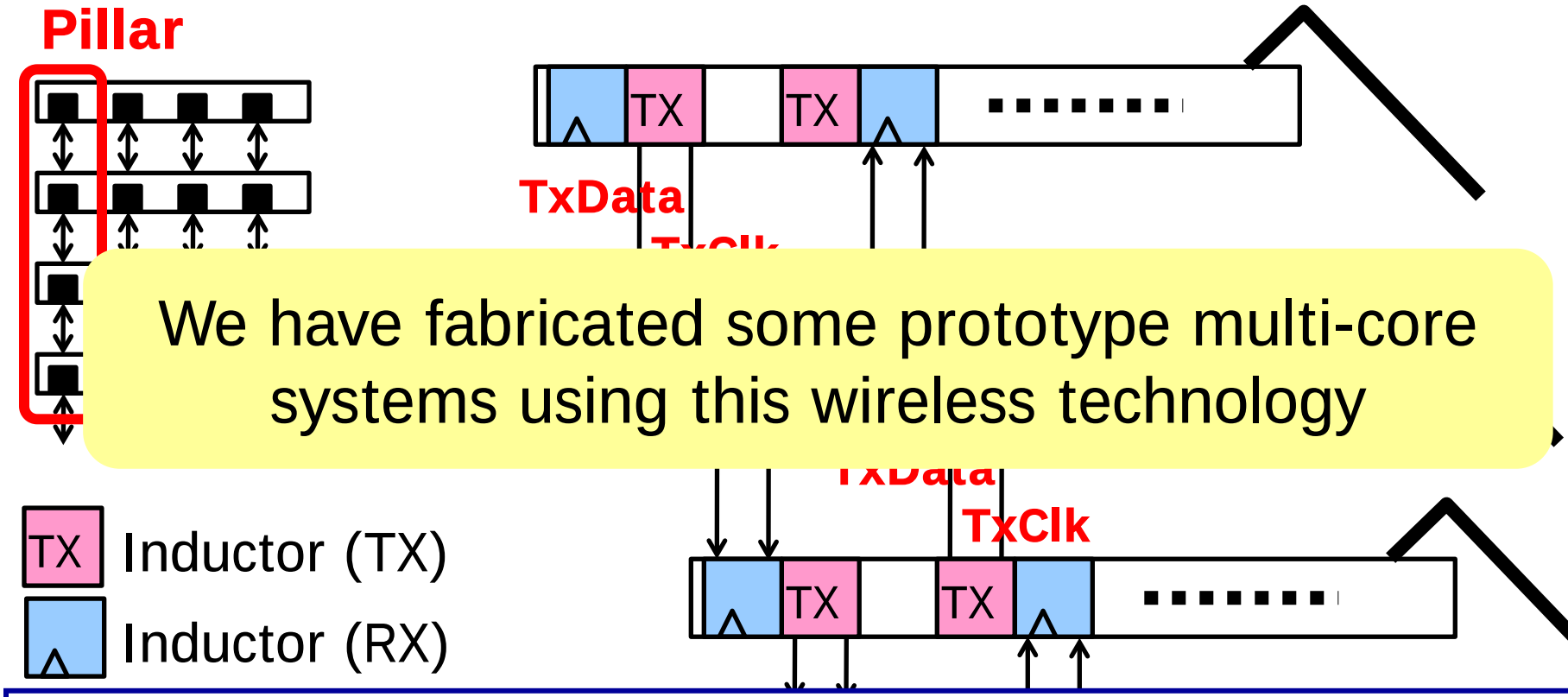
TX Inductor (TX)

Inductor (RX)

Stacking method: Staircase stacking

- Inductive-coupling link
  - Local clock @ 4GHz
  - Serial data

System clock for NoC: 200MHz
→ 35-bit transfer for each clock



We have fabricated some prototype multi-core systems using this wireless technology

Local clock shared by neighboring chips; No global sync.

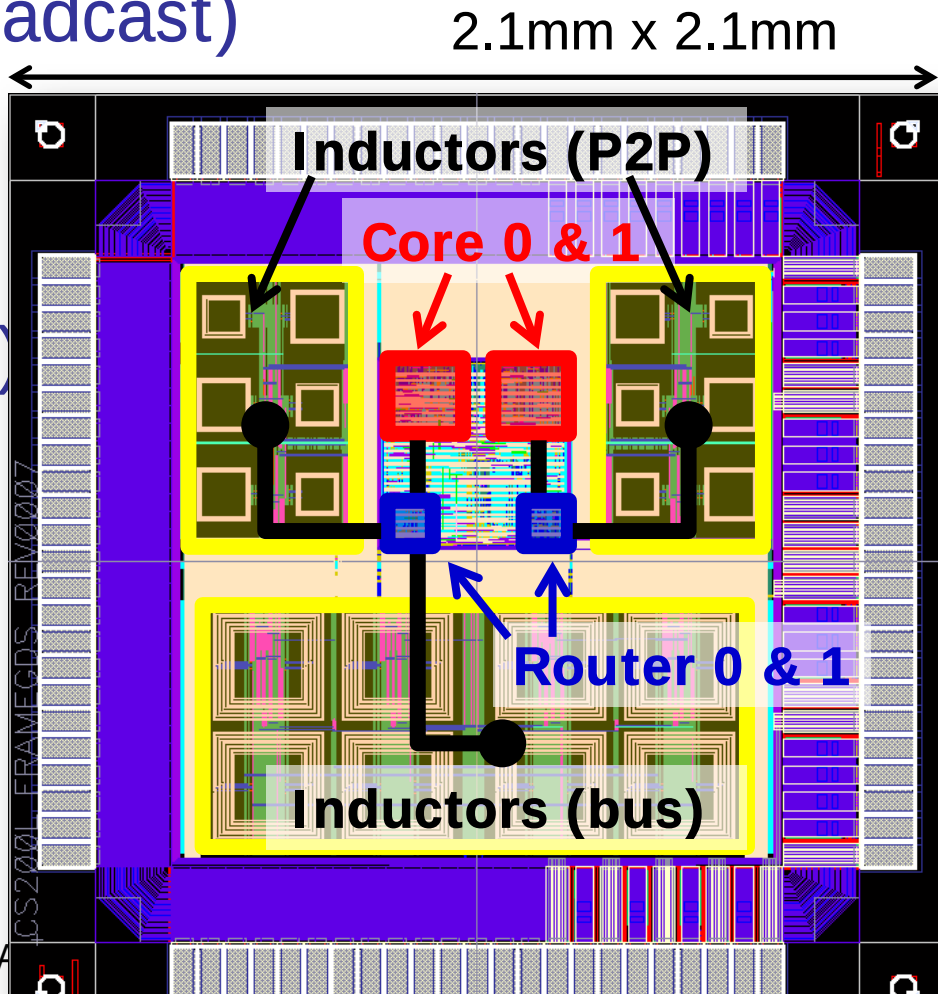
An example: Cube-0 (2010)

- Test chip for vertical communication schemes
  - Vertical point-to-point link between adjacent chips
  - Vertical shared bus (broadcast)

[Matsutani, NOCS'11]

- Each chip has
  - 2 cores (packet counter)
  - 2 routers
  - Inductors (P2P ring)
  - Inductors (vertical bus)

Process: Fujitsu 65nm (CS202SZ)
Voltage: 1.2V
System clock: 200MHz



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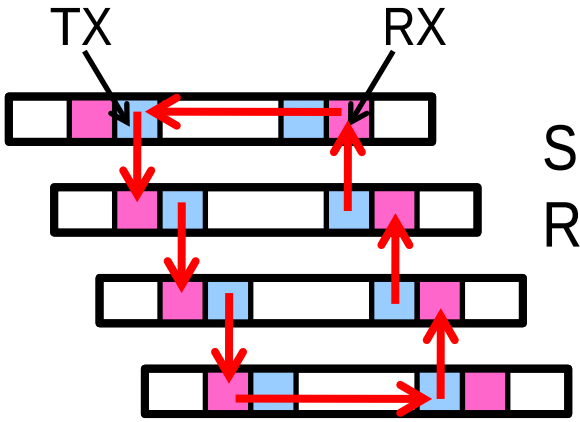
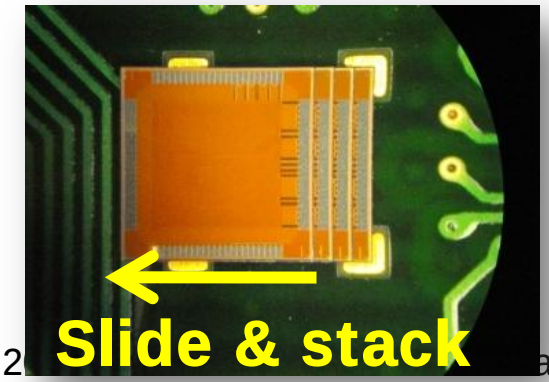
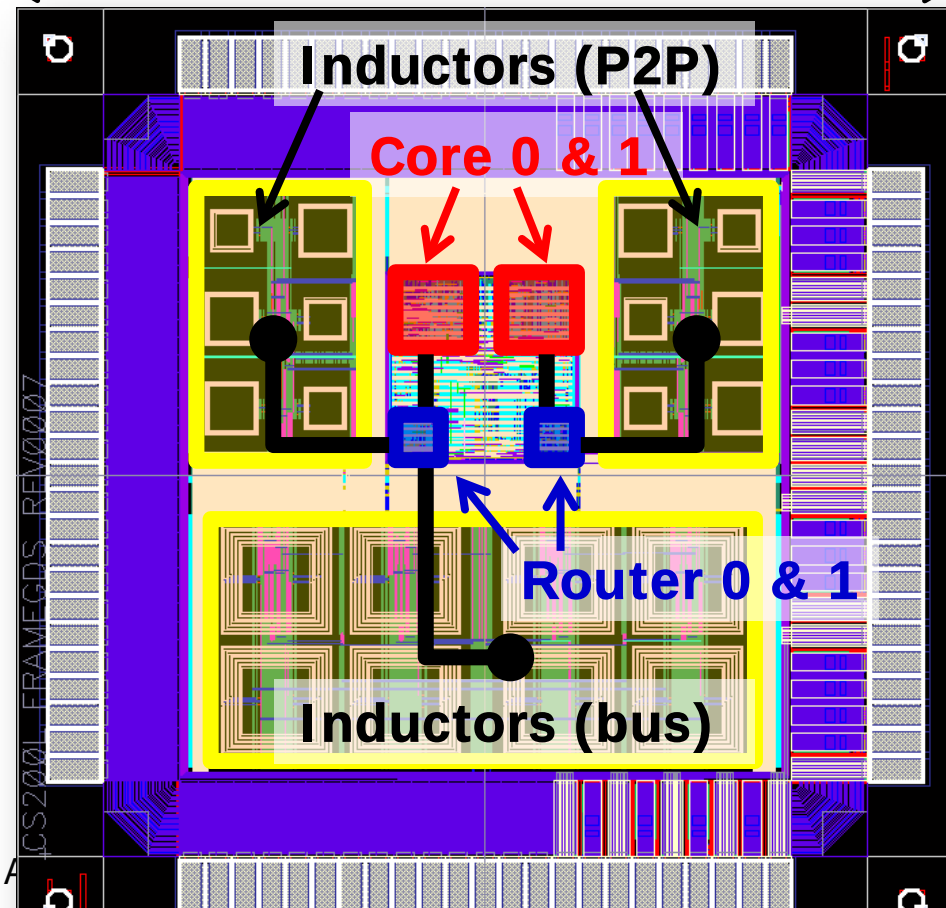
[Matsutani, NOCS'11]



Stacking for
Ring network



2.1mm x 2.1mm



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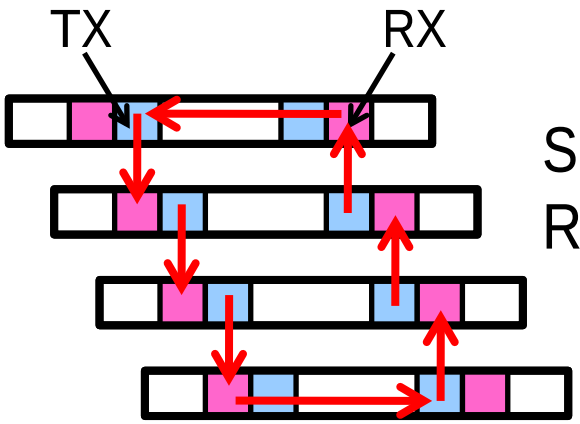
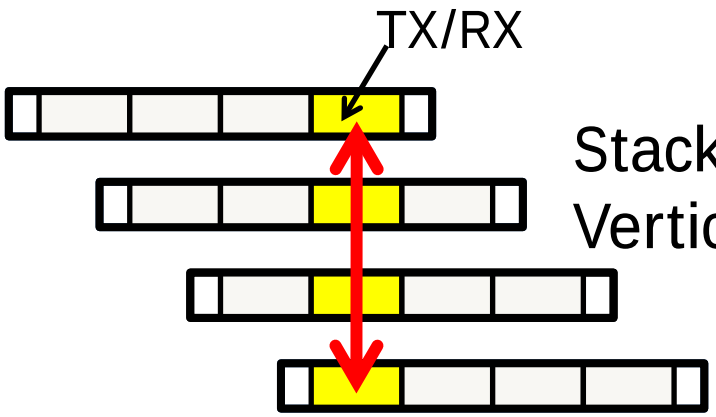
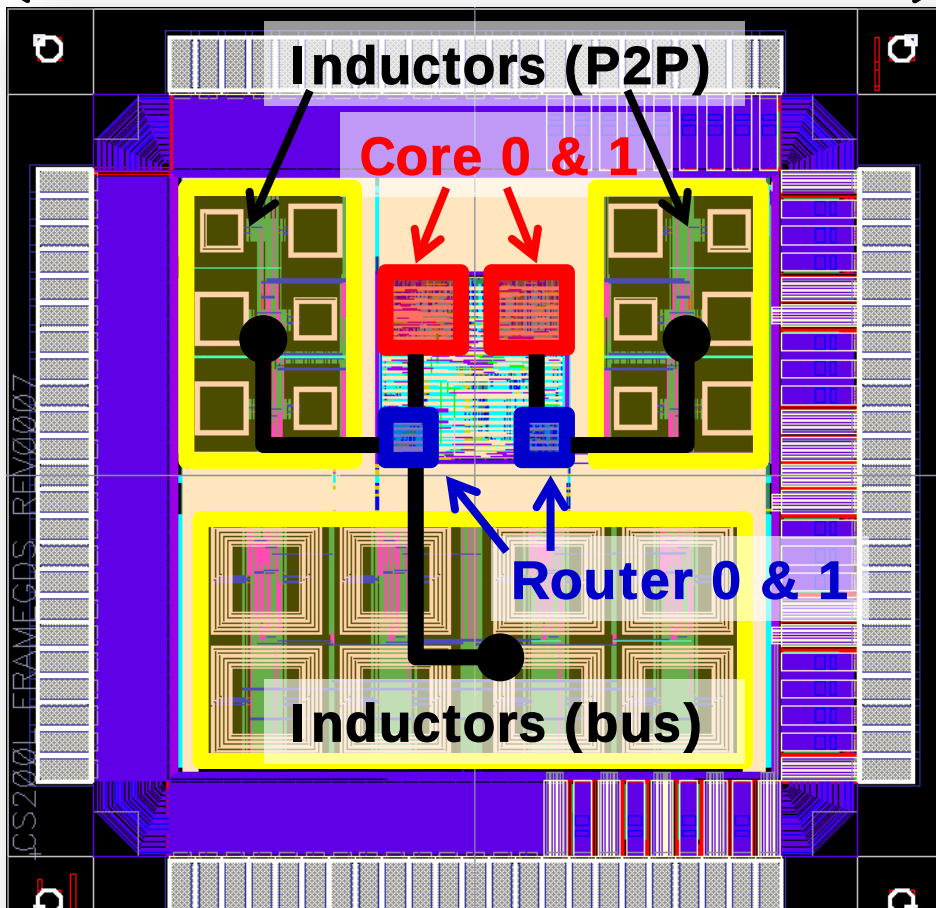


Stacking for Ring network



Stacking for Vertical bus

2.1mm x 2.1mm



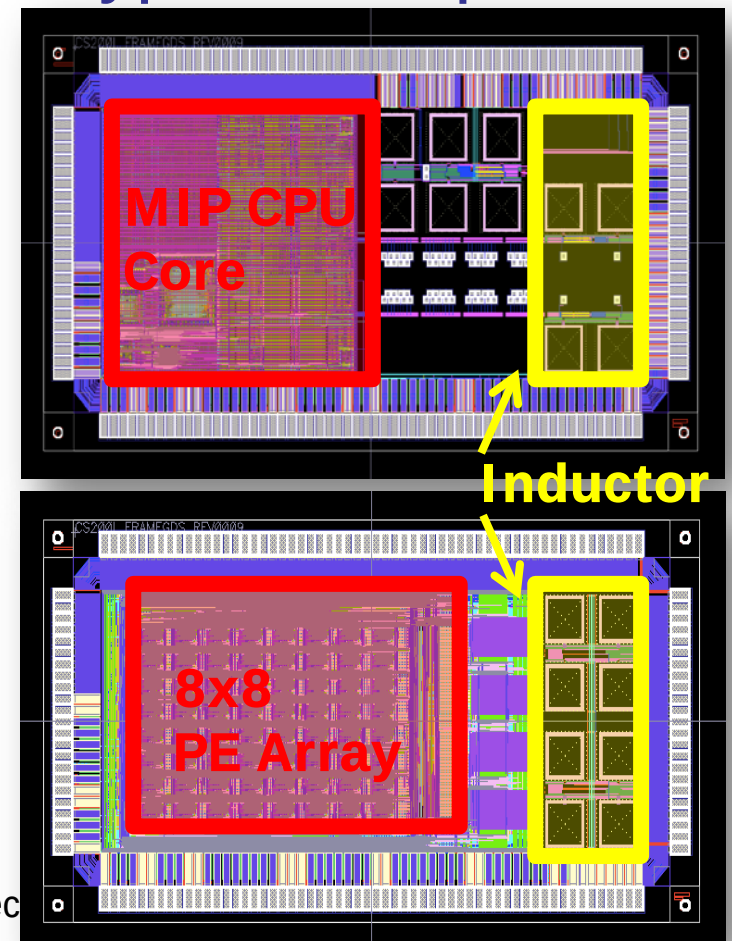
An example: Cube-1 (2012)

- Test chips for building-block 3D systems
  - Two chip types: Host CPU chip & Accelerator chip
  - We can customize number & types of chips in SiP

[Miura, IEEE Micro 13]

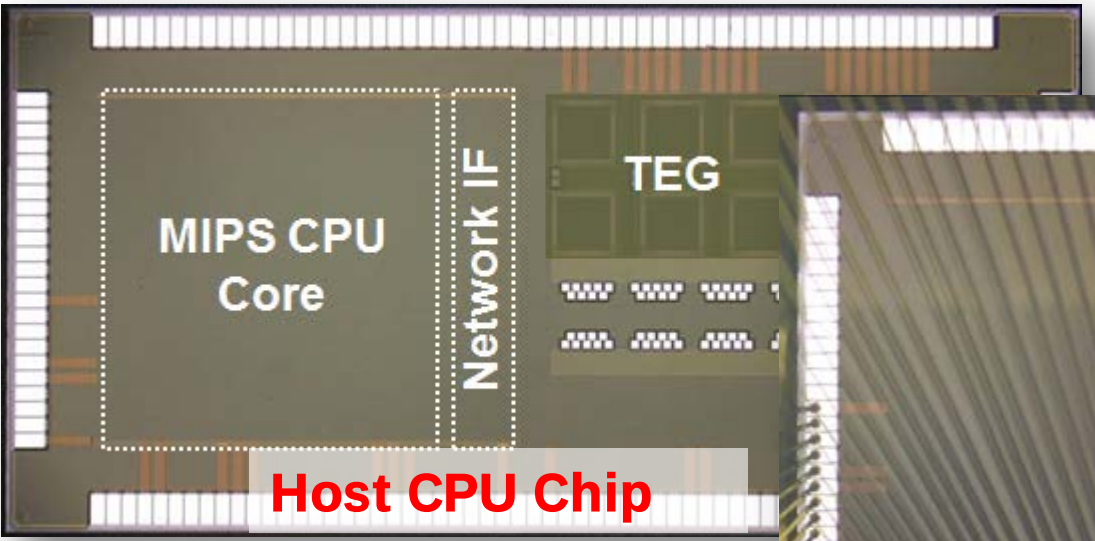
- Cube-1 Host CPU chip
  - Two 3D wireless routers
  - MIPS-like CPU

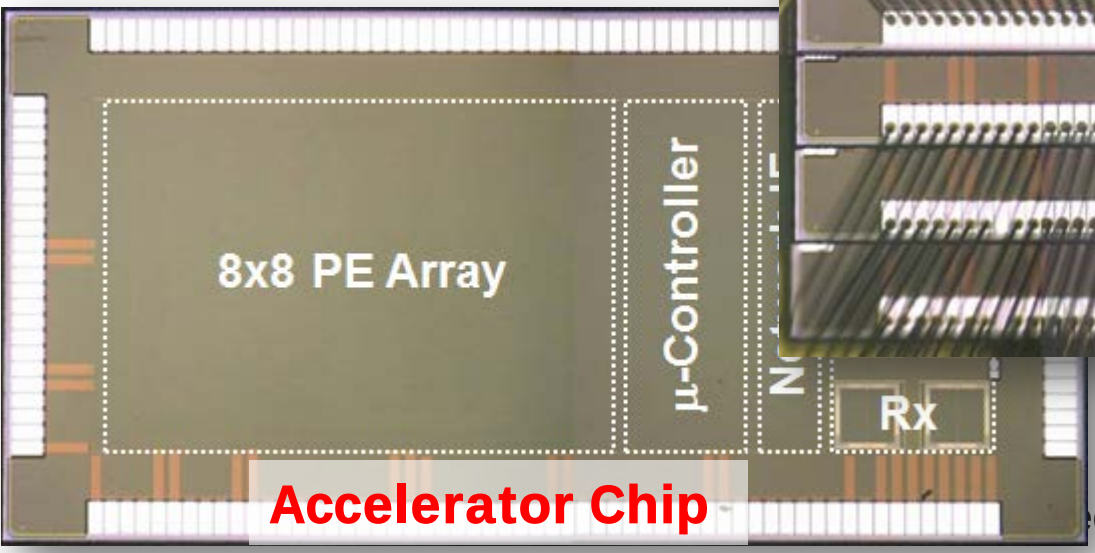
- Cube-1 Accelerator chip
  - Two 3D wireless routers
  - Processing element array



An example: Cube-1 (2012)

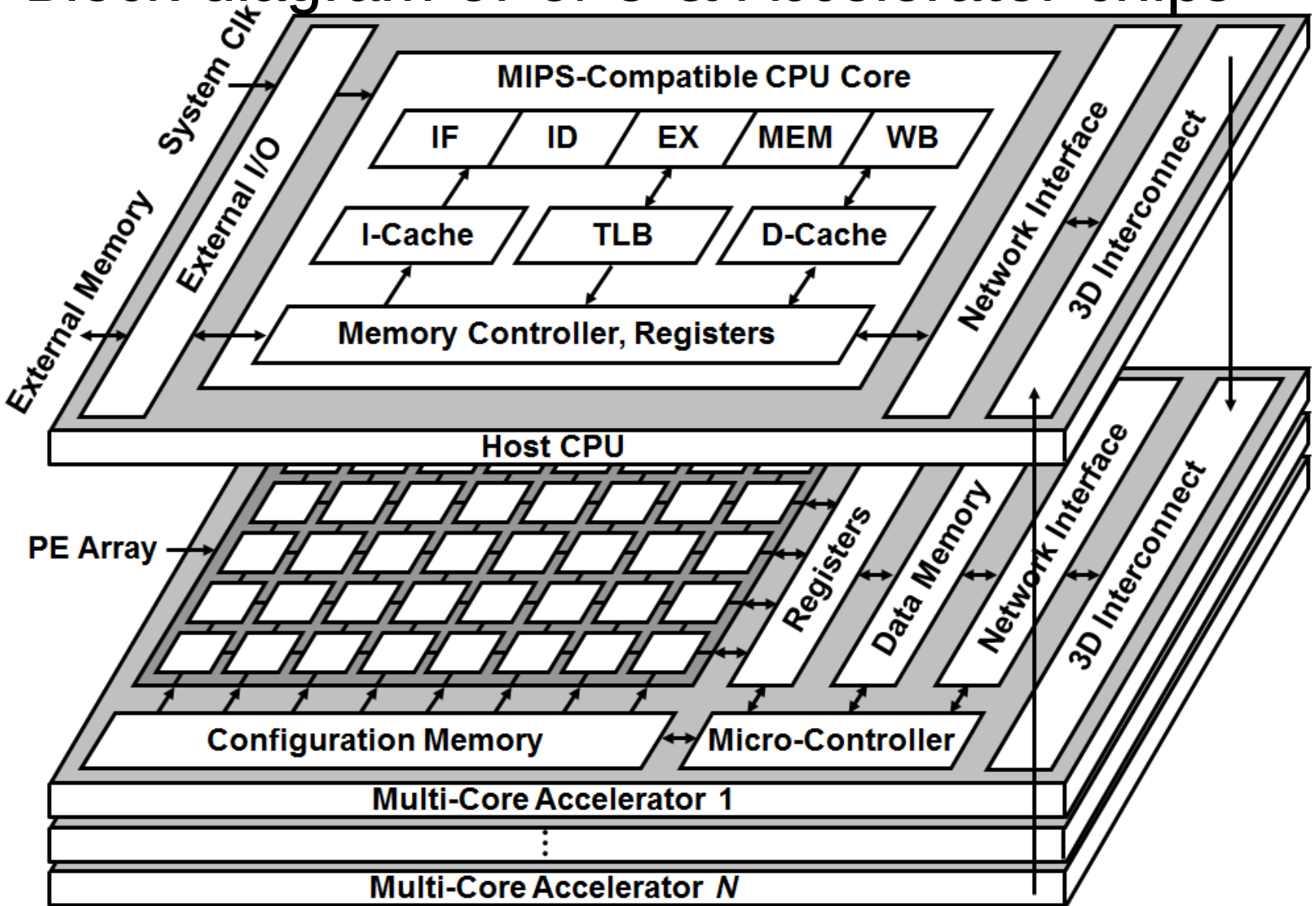
- Microphotographs of test chips [Miura, IEEE Micro 13]





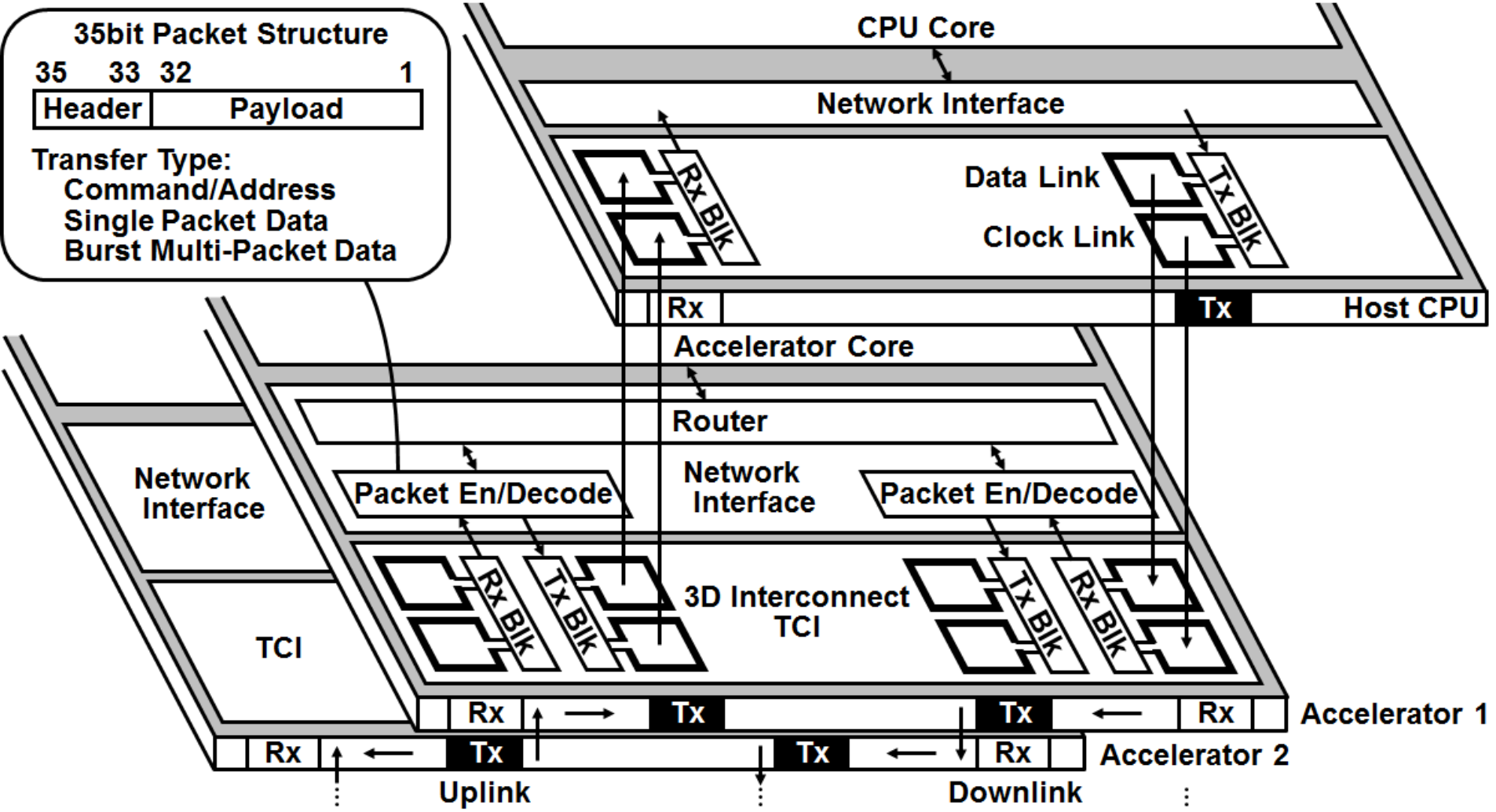
An example: Cube-1 (2012)

- Block diagram of CPU & Accelerator chips



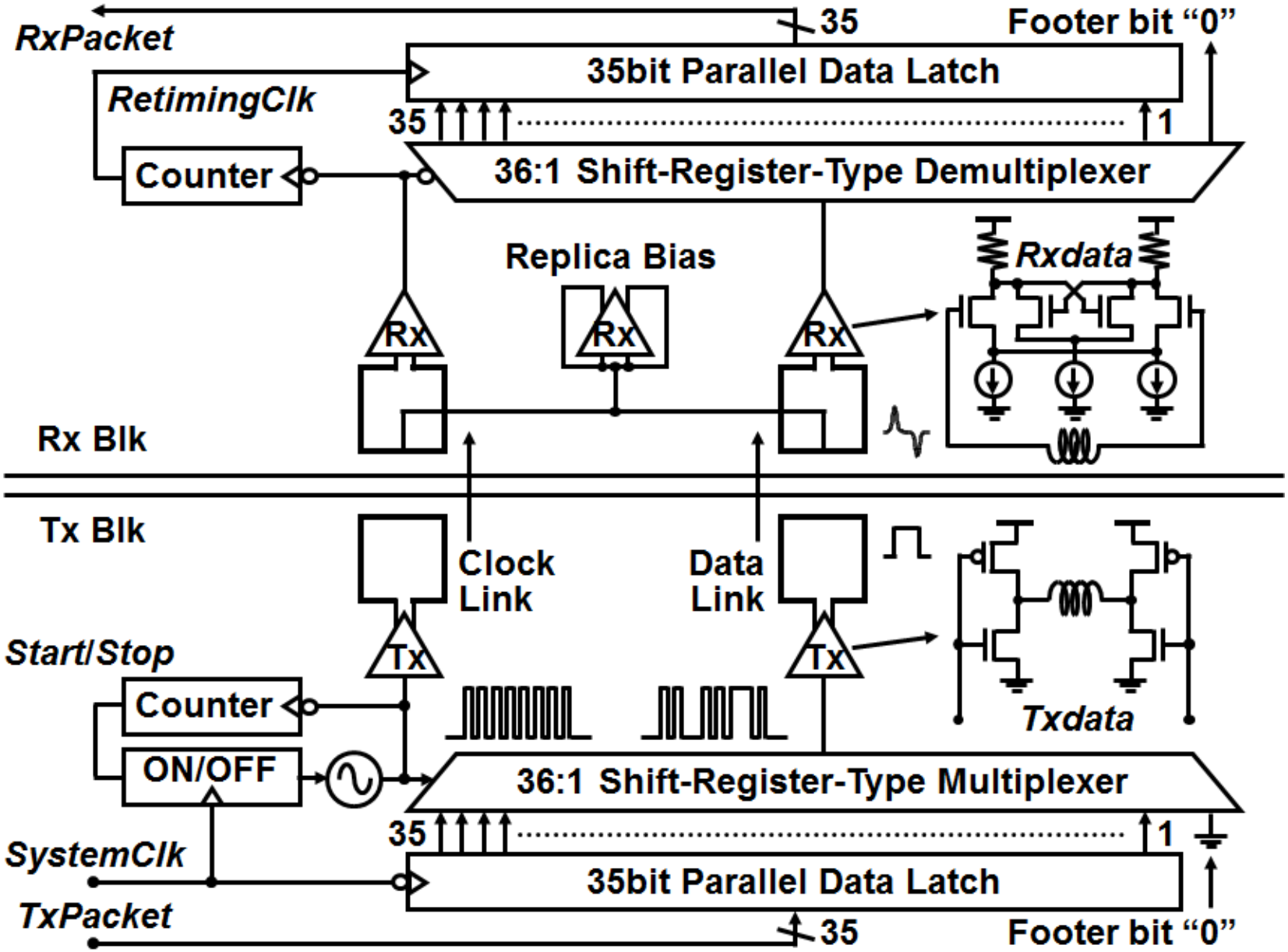
An example: Cube-1 (2012)

- Inductive-coupling ThruChip Interface (TCI)



Note: Please refer to Part III for antenna design for on-chip wireless.

An example: Cube-1 (2012)



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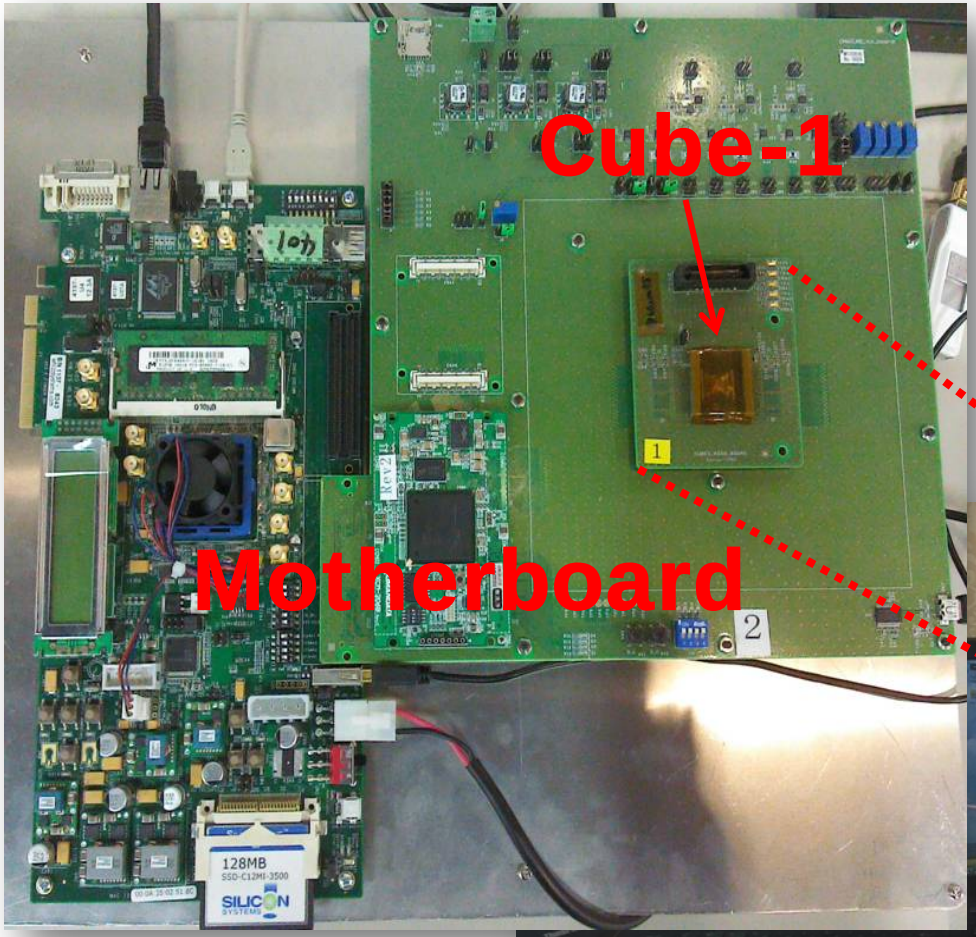
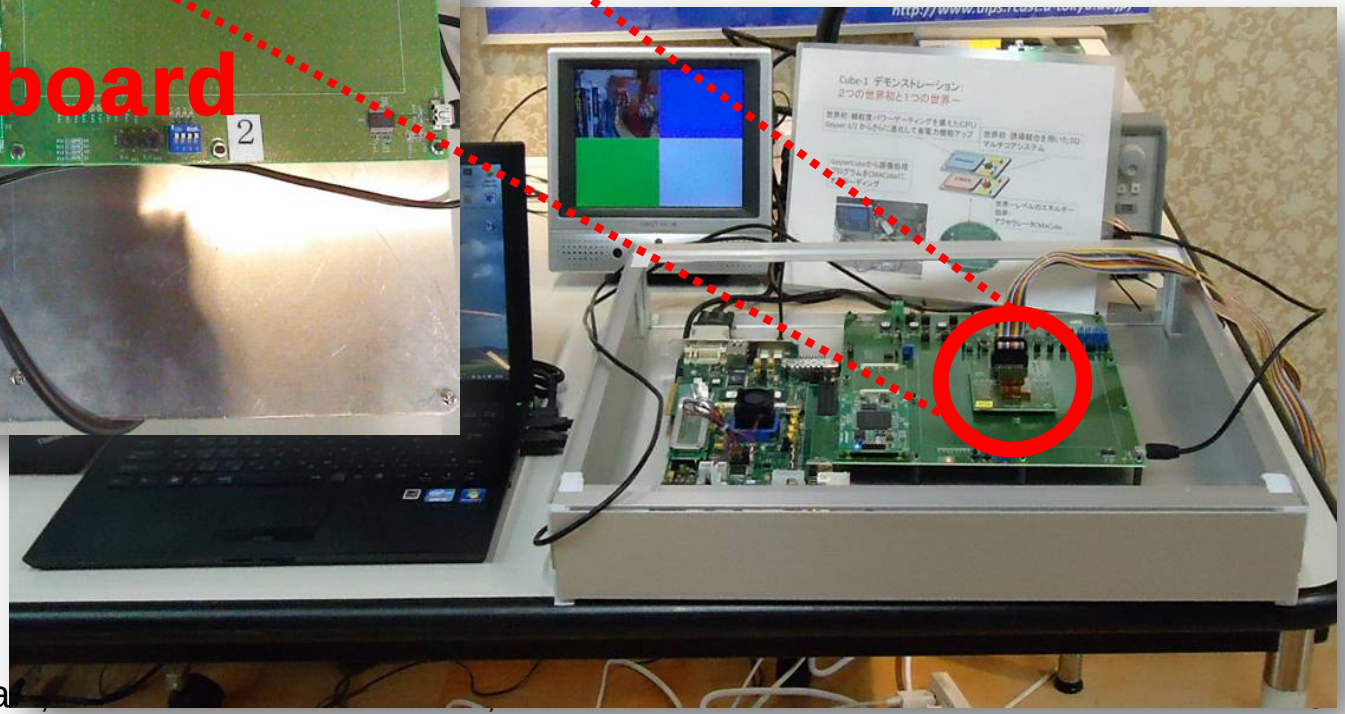


Cube-1 demo system

PE array chip performs image processing

CPU chip for control

[Miura, HotChips'13 Demo]



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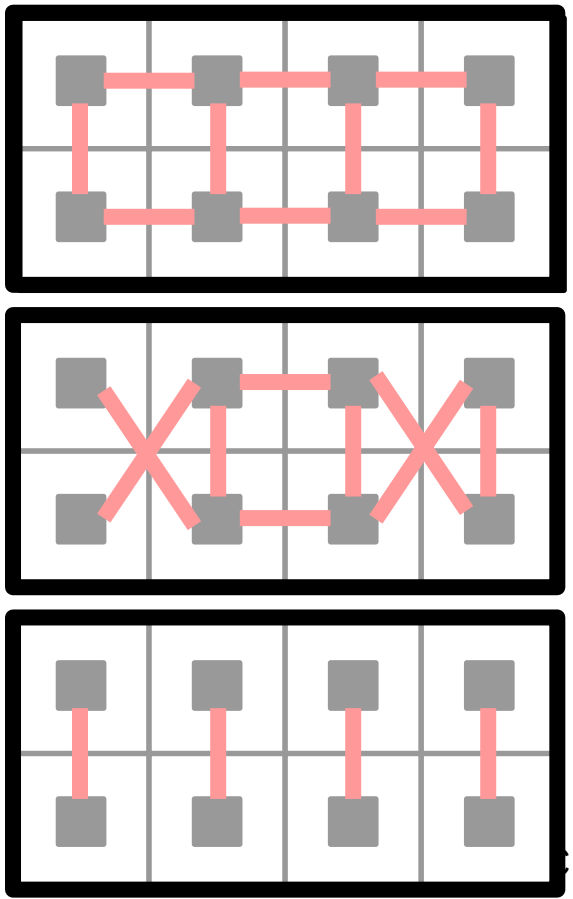
Big picture: Wireless 3D NoC

- Arbitrary chips are stacked after fabrication
  - Each chip has vertical links at pre-specified locations, but we do not know internal topology of each chip
  - Wireless 3D NoC required to stack unknown topologies



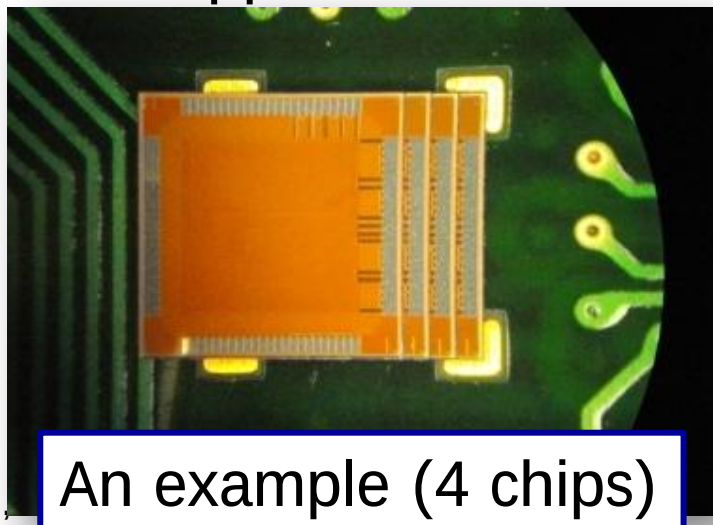
Memory chip from A

GPU chip from B

CPU chip from C

Note: We can add long-range links to induce small-world effects [See Part I]

Required chips are stacked for each application



An example (4 chips)

Two approaches: Wireless 3D NoC arch

Chips should be added, removed, swapped for each app.

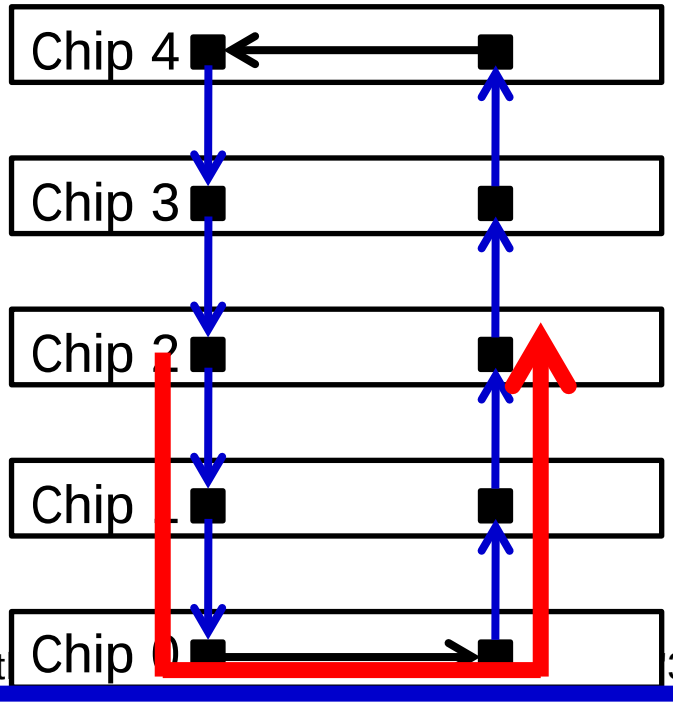
- Ring-based approach

Good Easy to add & remove

Bad – Inefficient hop count

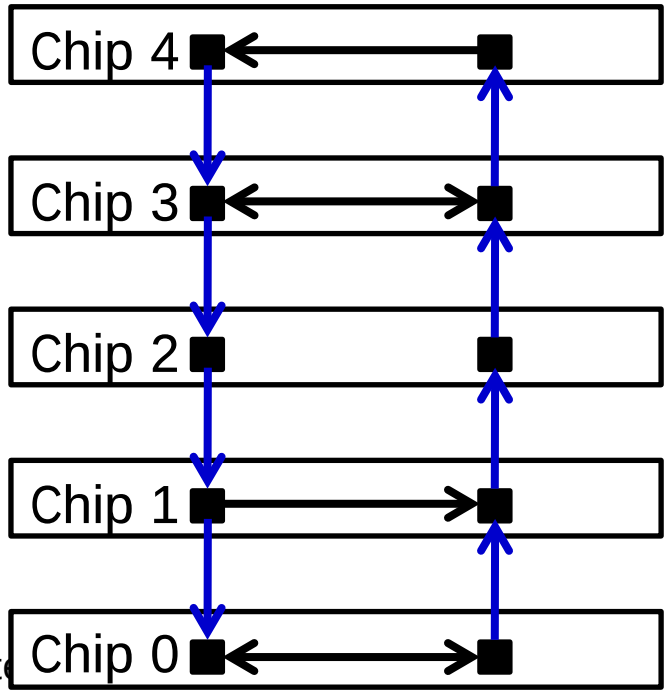
Bad – No scalability

[Matsutani, NOCS'11]



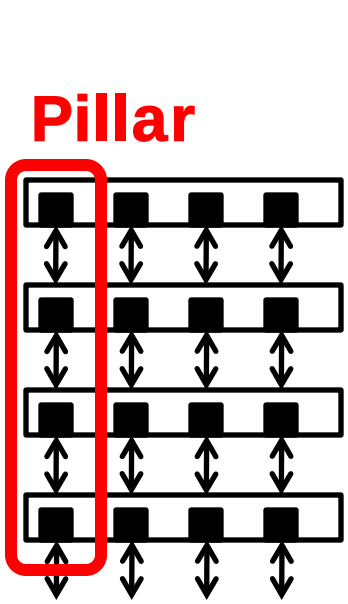
- Irregular approach
  - We can use any links
  - Irregular routing needed
  - Plug-and-play protocol

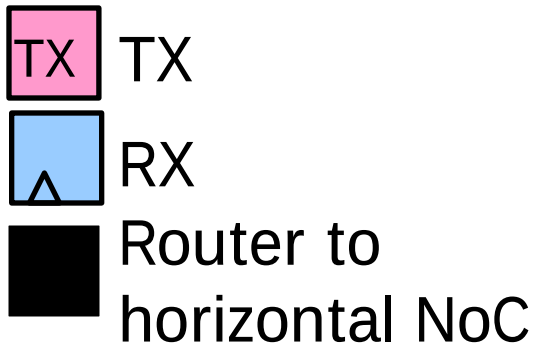
[Matsutani, ASPDAC'13]

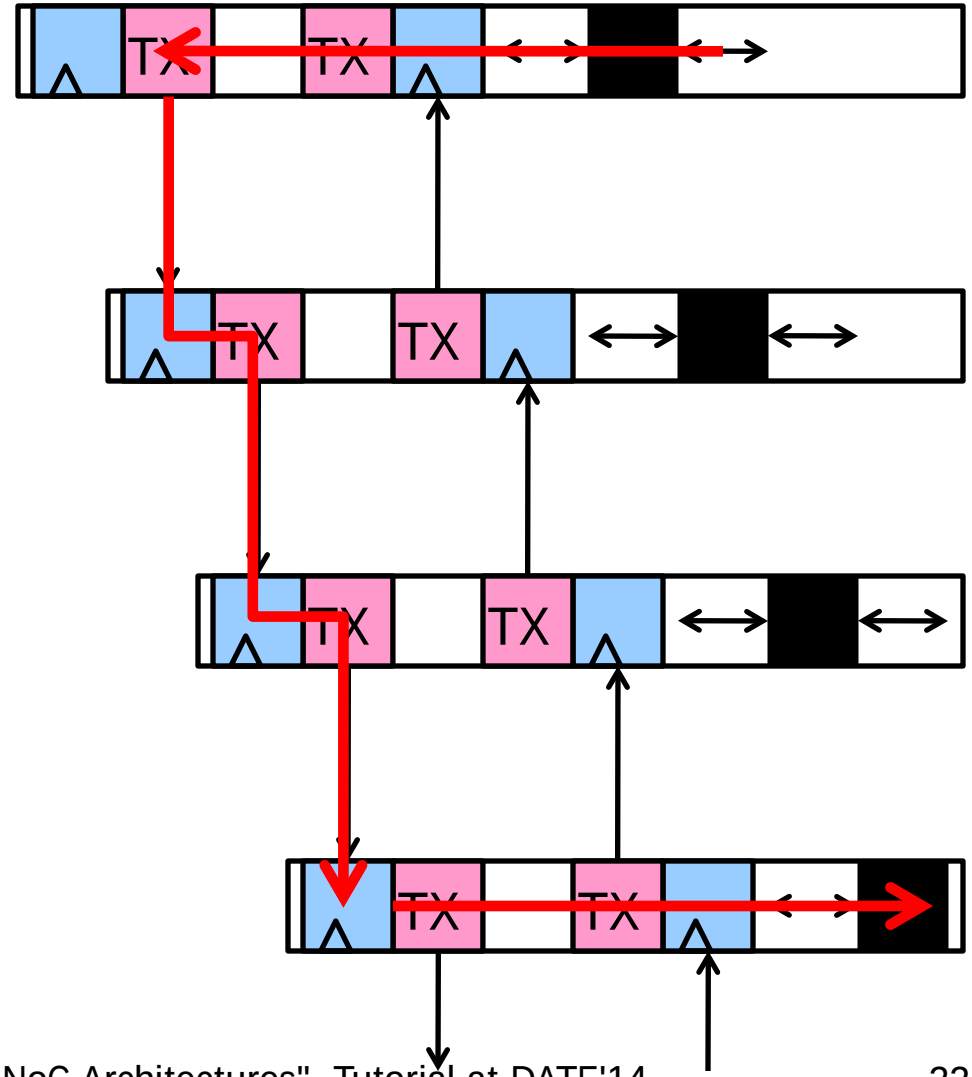


Ring-based 3D wireless NoC

- Chips are connected via unidirectional rings

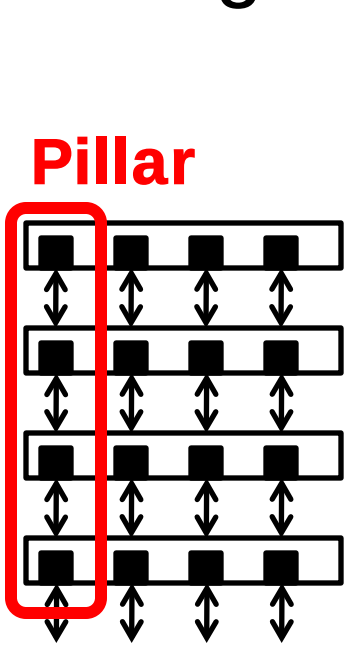


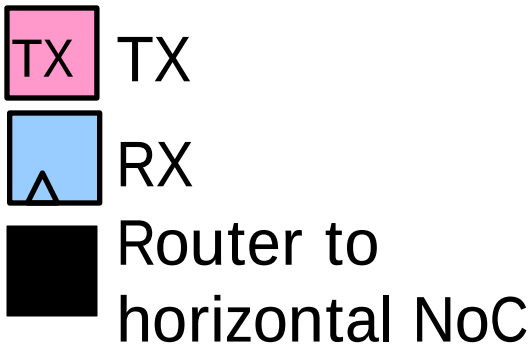


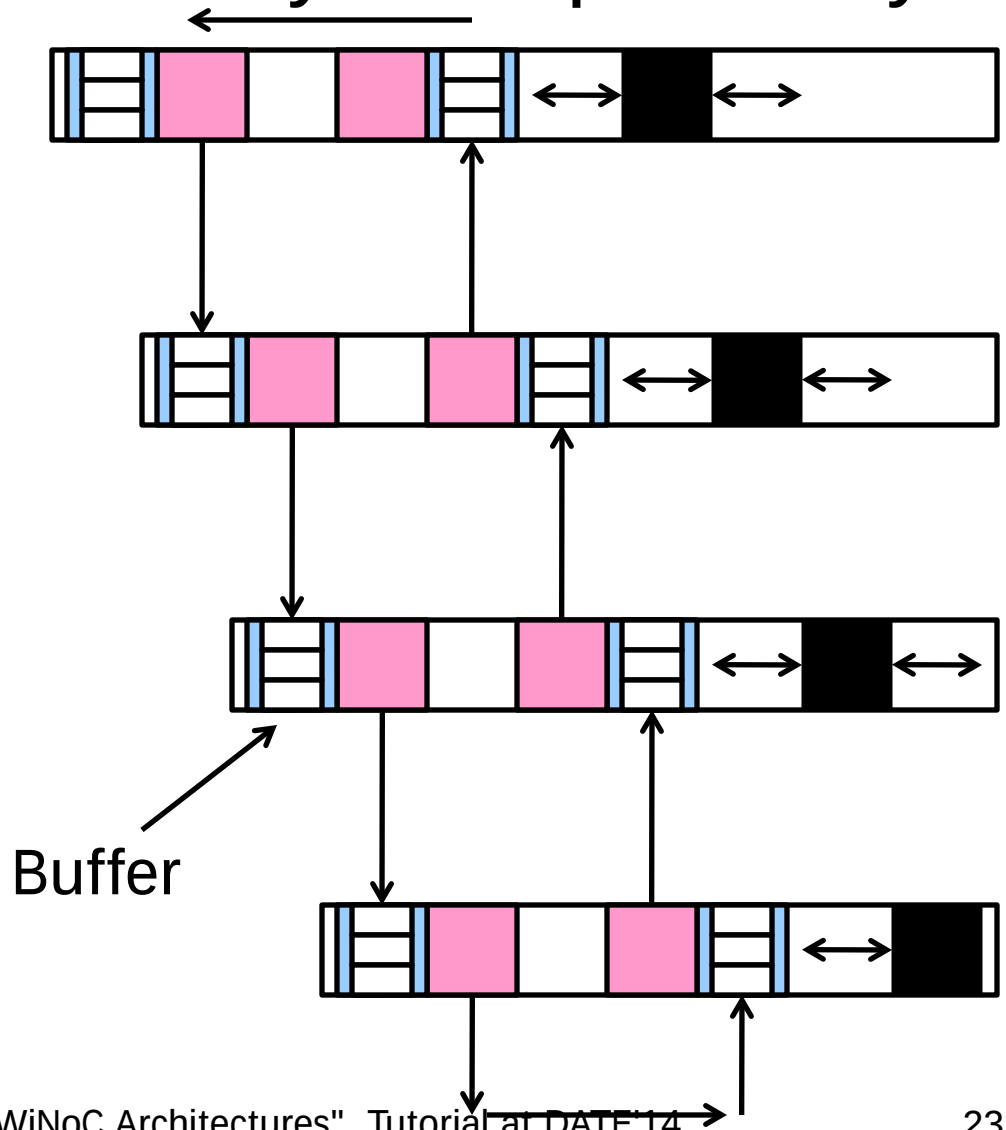


Ring approach: Deadlock problem

- Ring inherently includes a cyclic dependency







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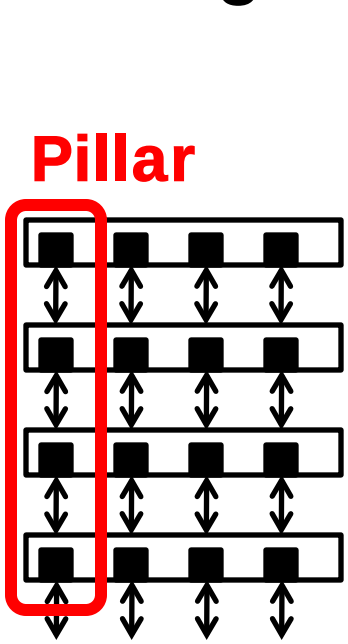

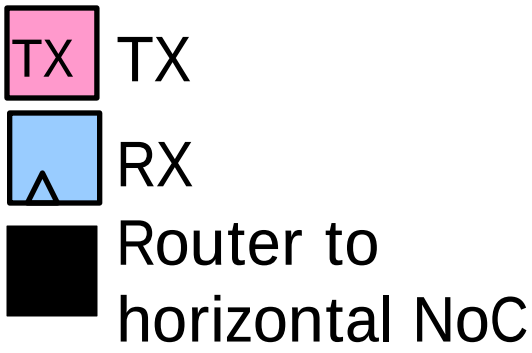

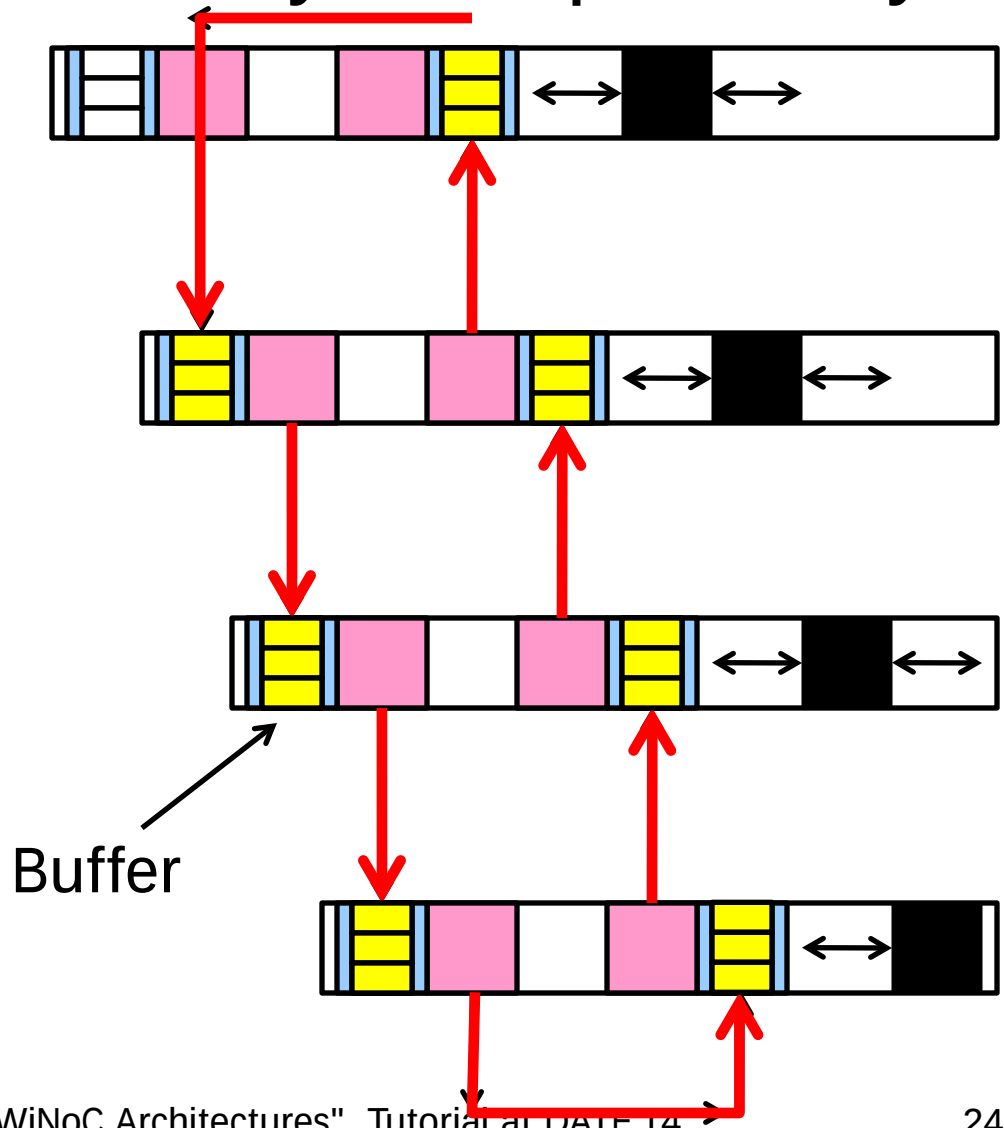

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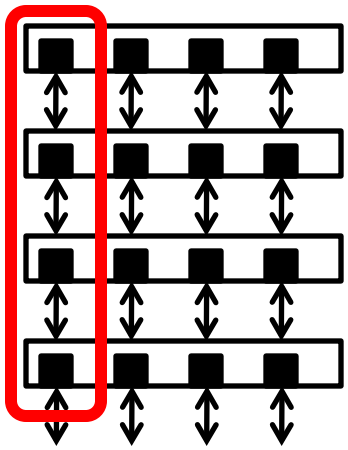
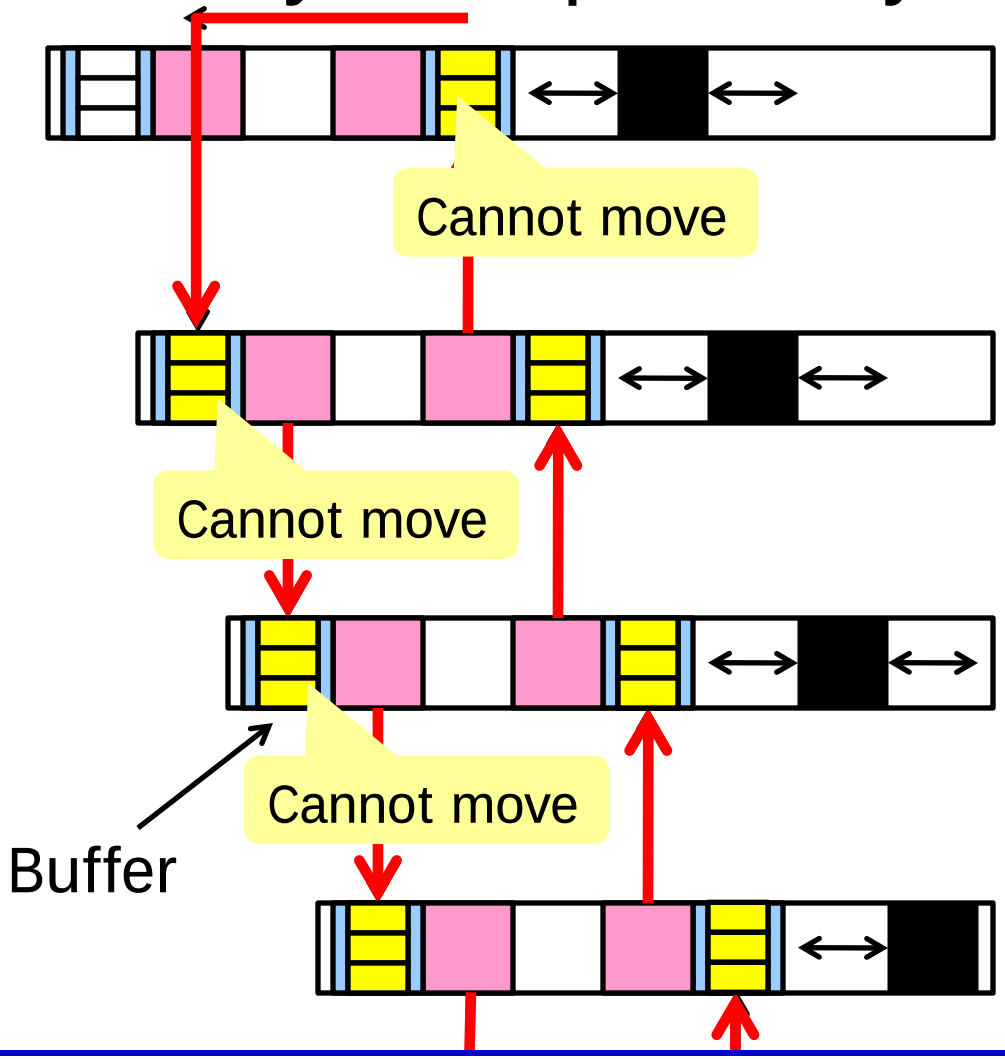


TX

RX

Router to horizontal NoC

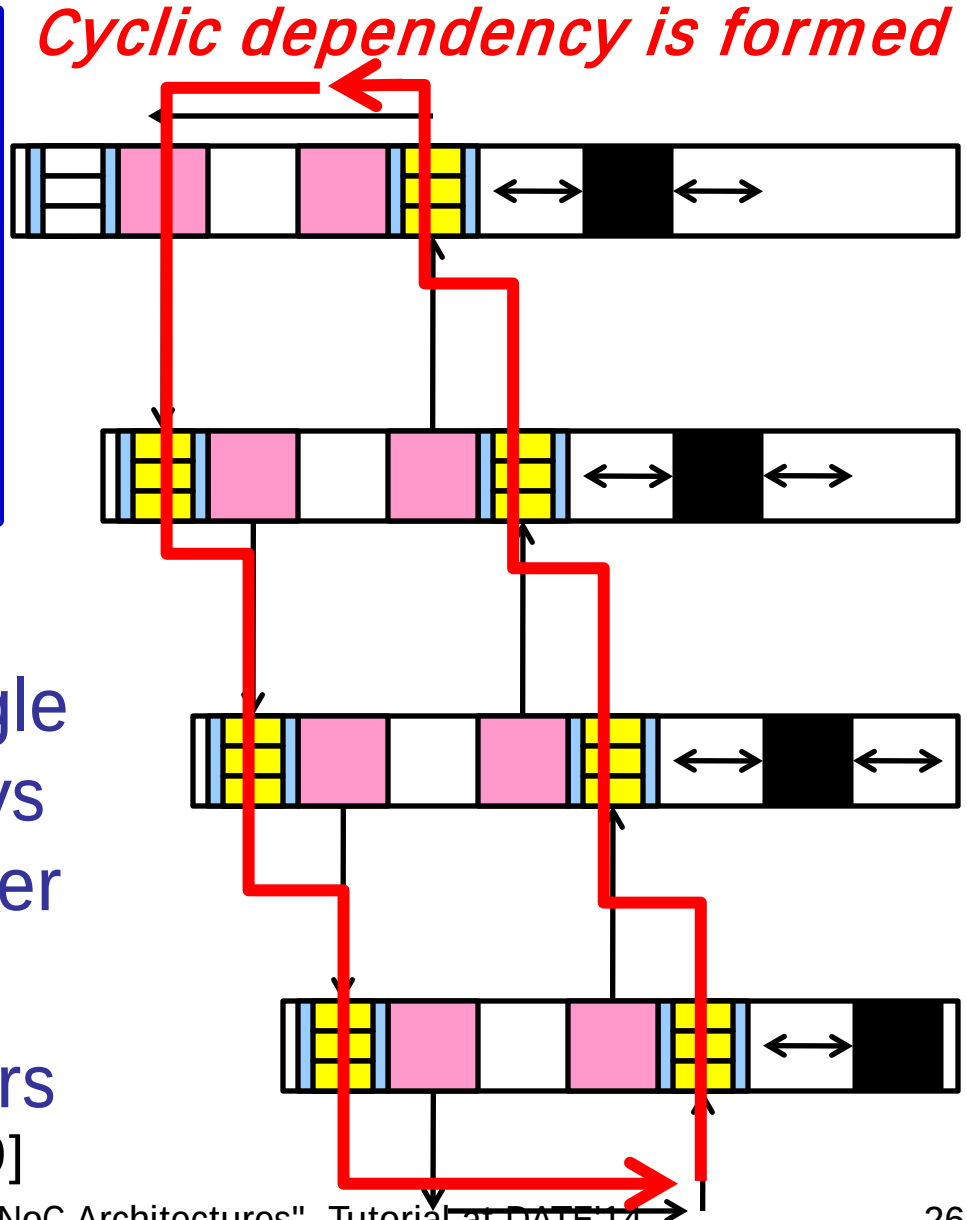


Any packets cannot advance → Deadlock avoidance is needed

Ring approach: Deadlock avoidance

- Adding extra VCs
  - Conventional way
  - Duplicating buffers
  - 2 VCs for each message class
- Bubble flow control
  - Buffer space of a single packet must be always reserved in each router
  - All message classes share the same buffers

[Puente,ICPP'99]



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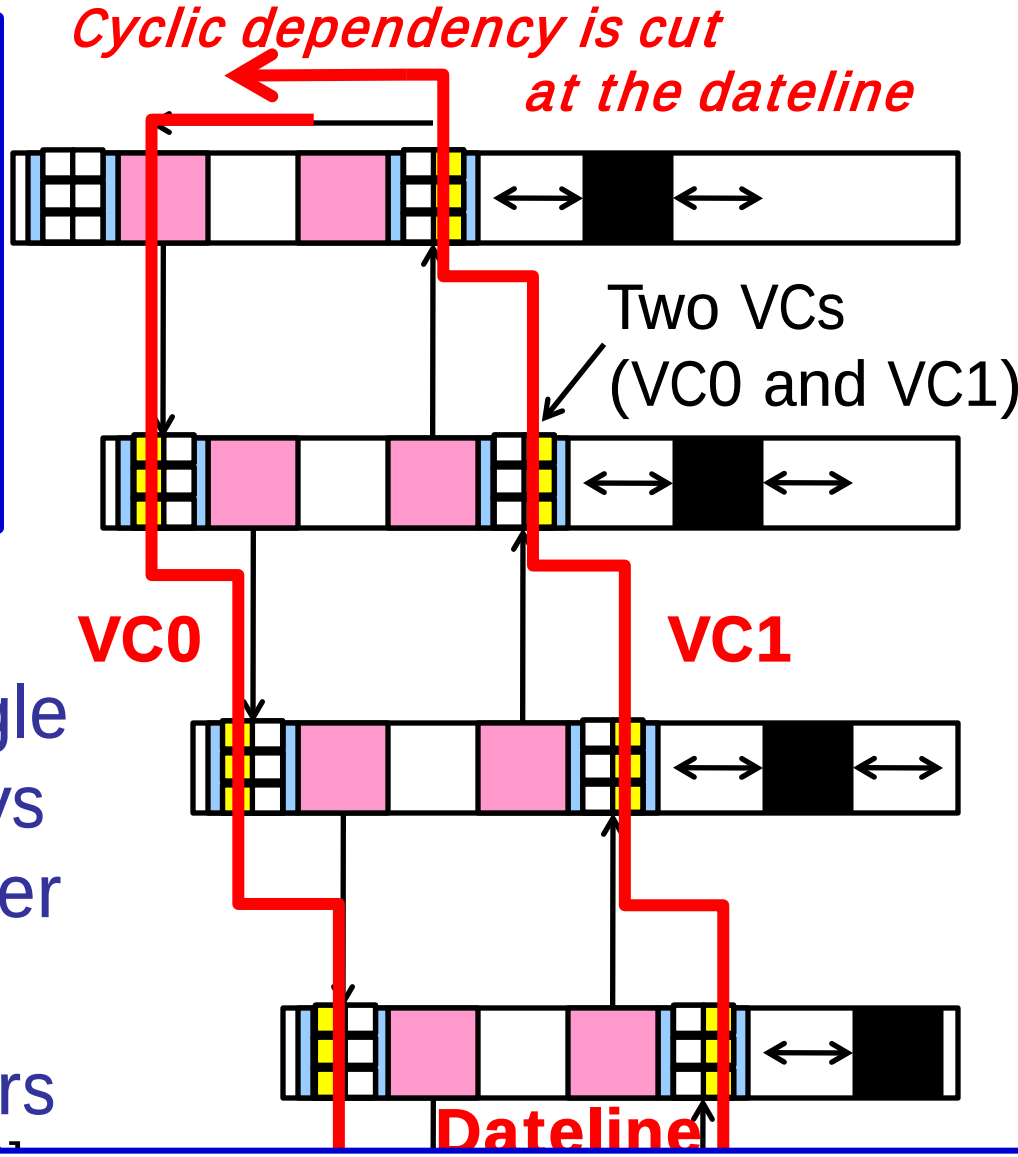

2 VCs required for a message class; Multi-core uses multiple classes

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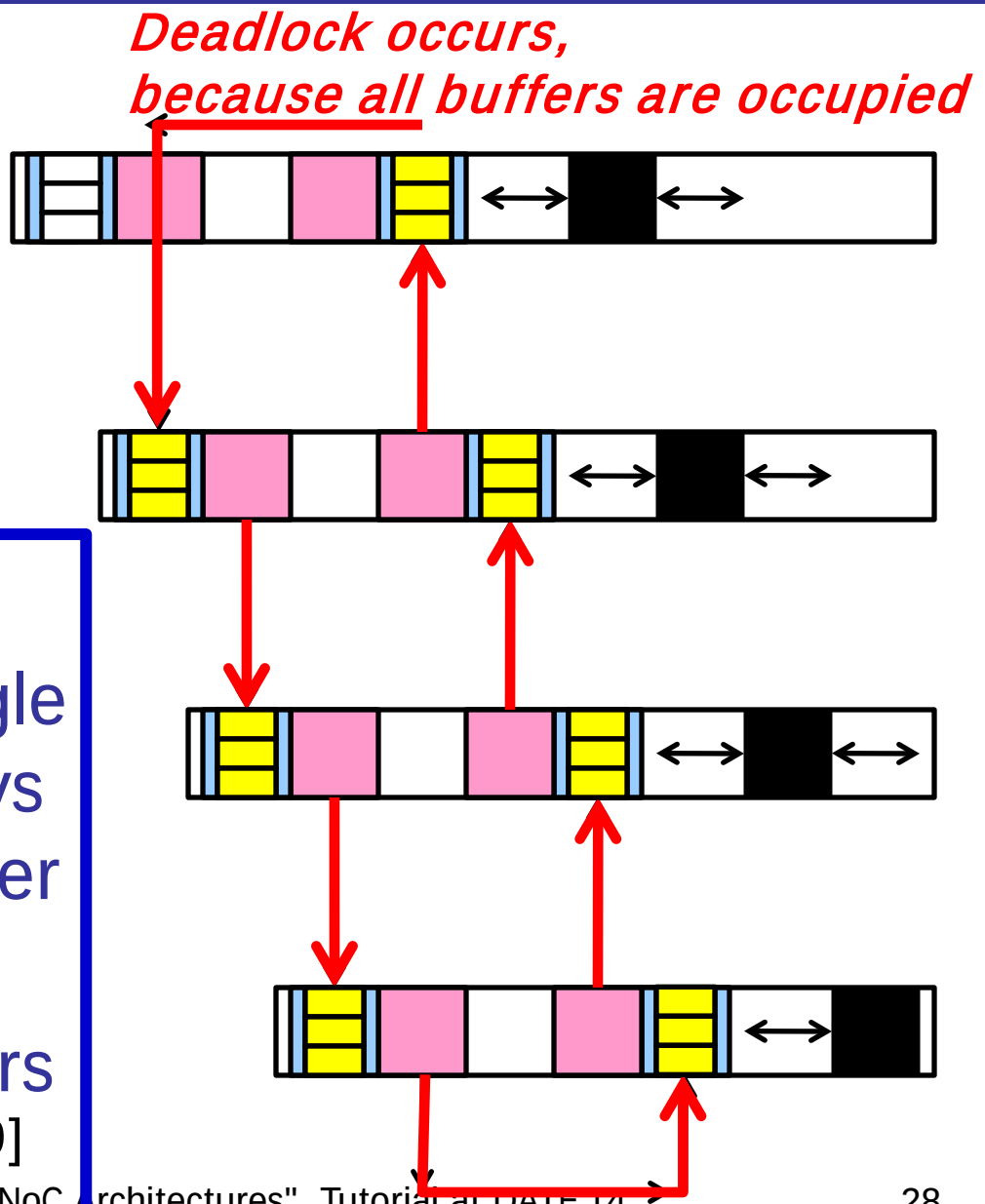

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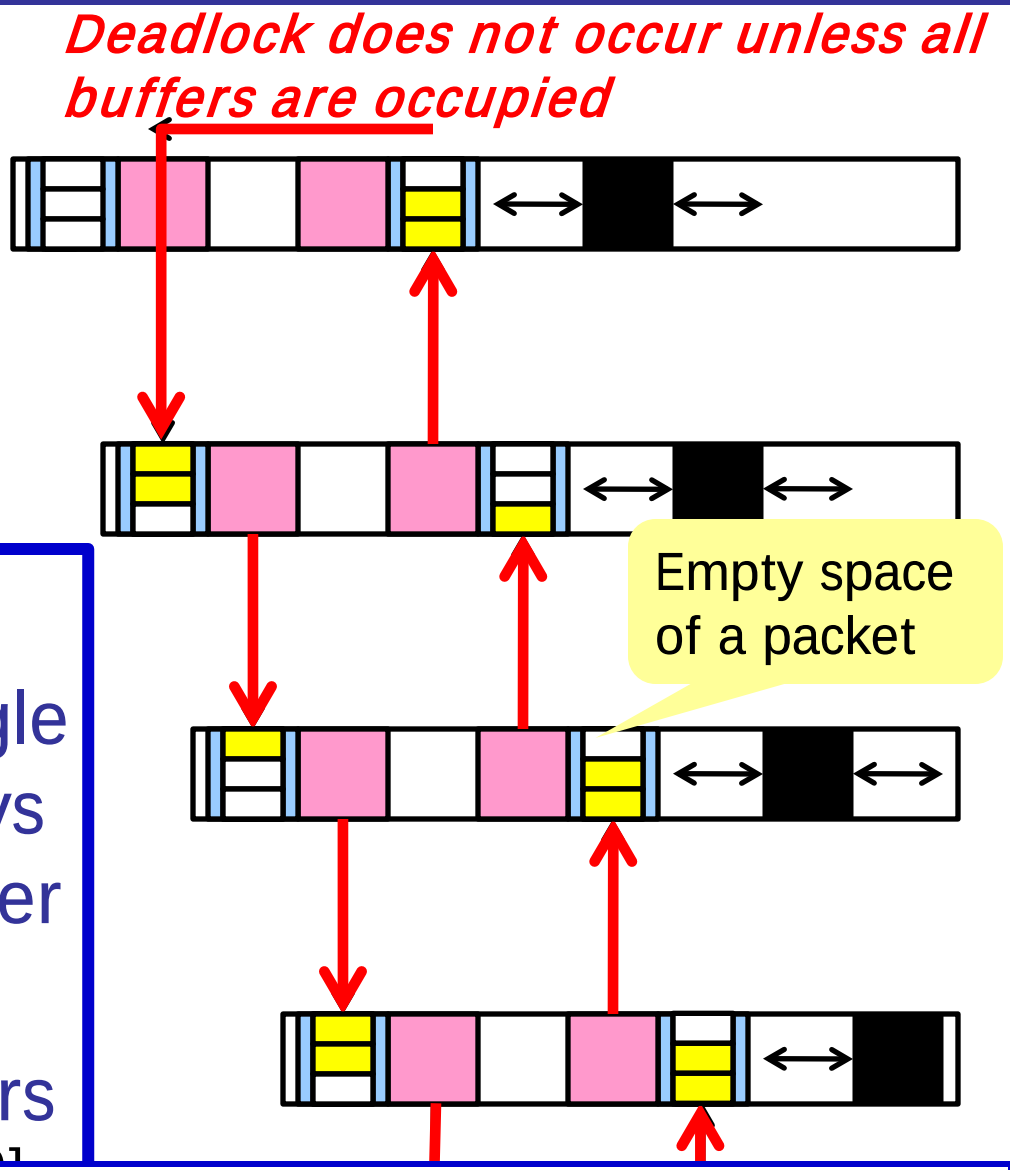
[Bubble, ICPP'00]



We employ Bubble flow for CMP with multiple message classes

Outline: 3D WiNoC Architectures

So far we focused on 2D WiNoC architecture and its physical link design. This part explores 3D WiNoC architectures, especially inductive-coupling 3D option.

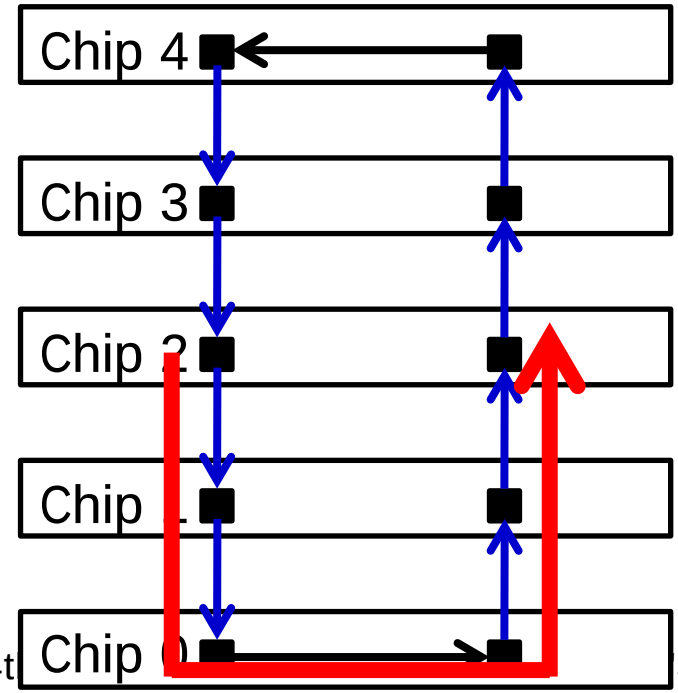
- 3D IC technologies: Wired vs. Wireless [5min]
- Prototype systems: Cube-0 & Cube-1 [15min]
- Wireless 3D NoC architectures [15min]
  - Ring-based 3D WiNoC
  - Irregular 3D WiNoC
- Experiment results and Summary [10min]

Two approaches: Wireless 3D NoC arch

Chips should be added, removed, swapped for each app.

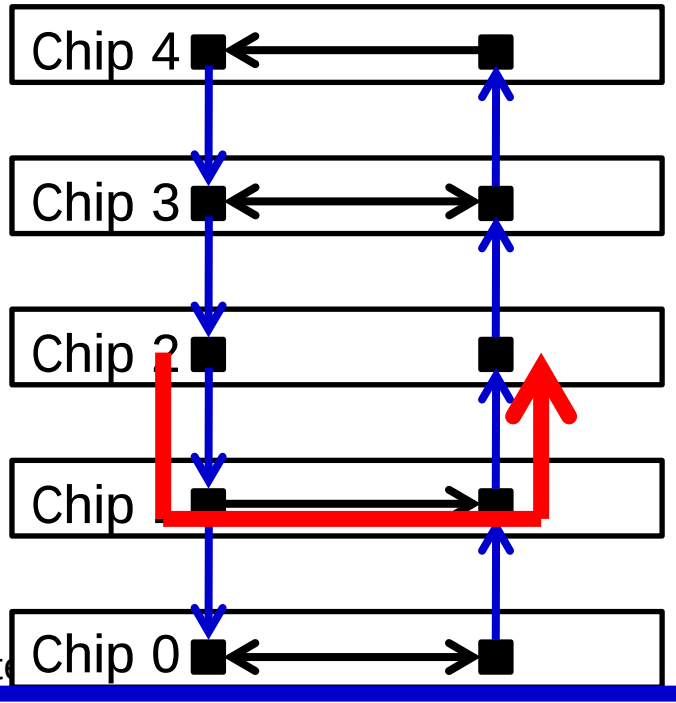
- Ring-based approach
  - Good – Easy to add & remove
  - Bad – Inefficient hop count
  - Bad – No scalability

[Matsutani, NOCS'11]



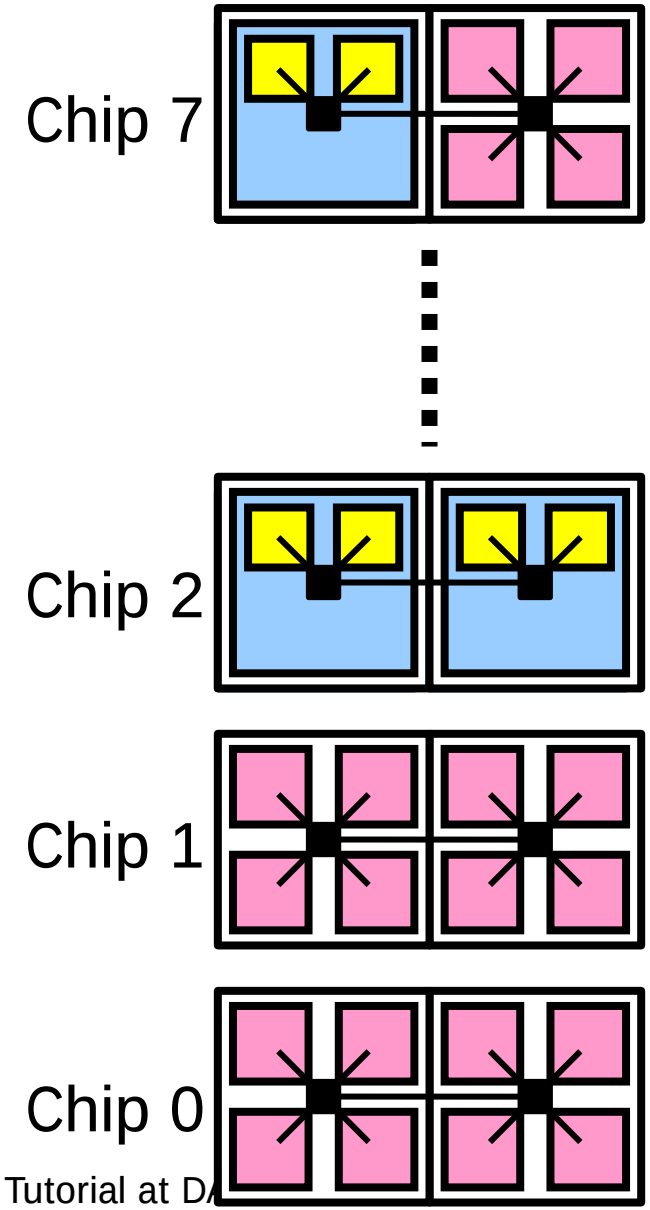
- Irregular approach
  - Good – We can use any links
  - – Irregular routing needed
  - – Plug-and-play protocol

[Matsutani, ASPDAC'13]



Irregular approach: Ad-hoc topology

- Wireless 3D CMPs
  - Various chips are stacked, depending on the application
- Each chip
  - Must have vertical links
  - May not have horizontal links
  - May have VCs for horizontal
- Ad-hoc wireless 3D NoC
  - We cannot expect the network topology, number of VCs, and its bandwidth before stacking



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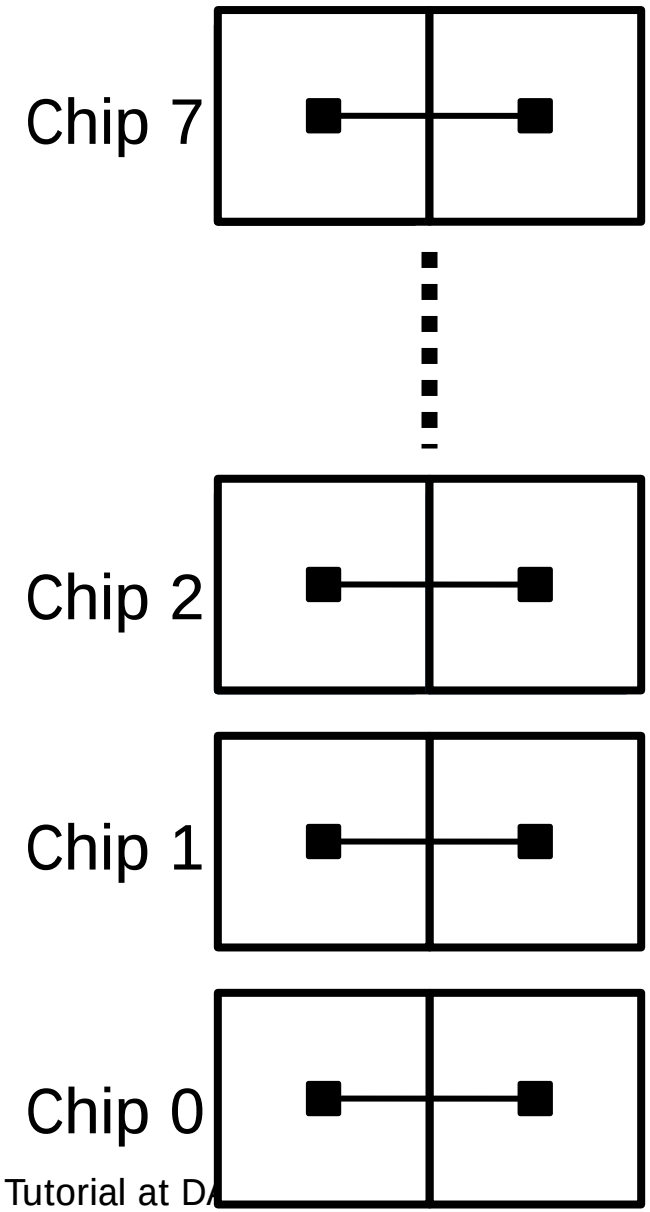

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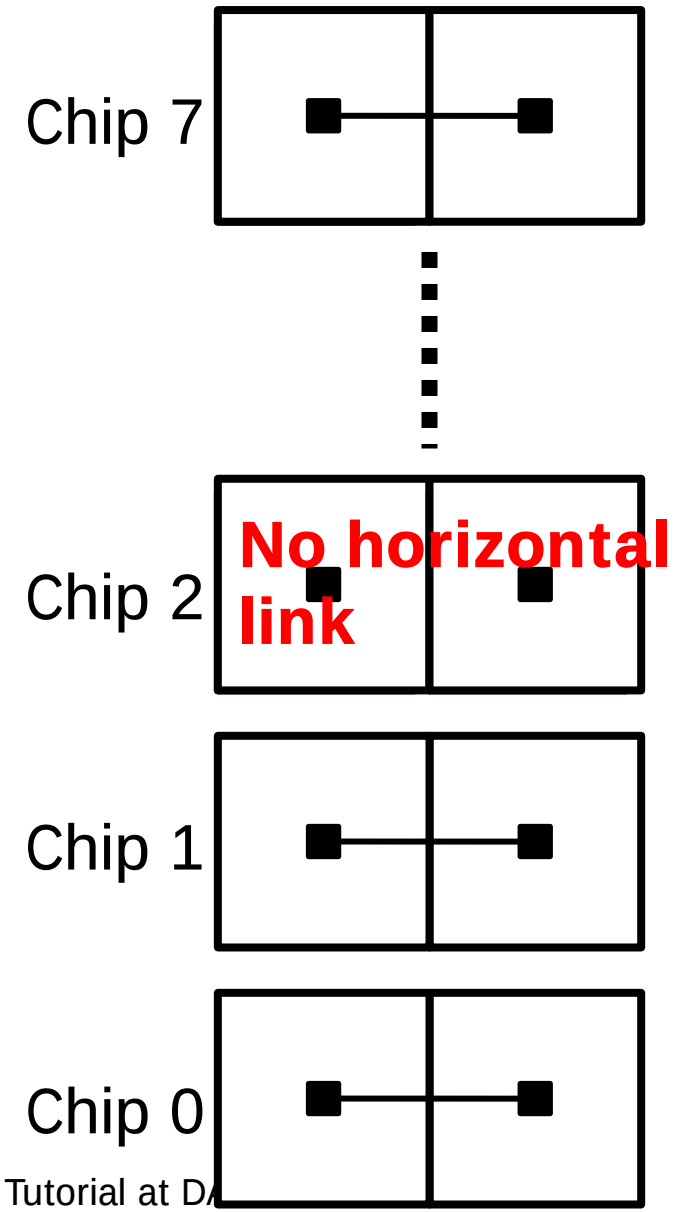

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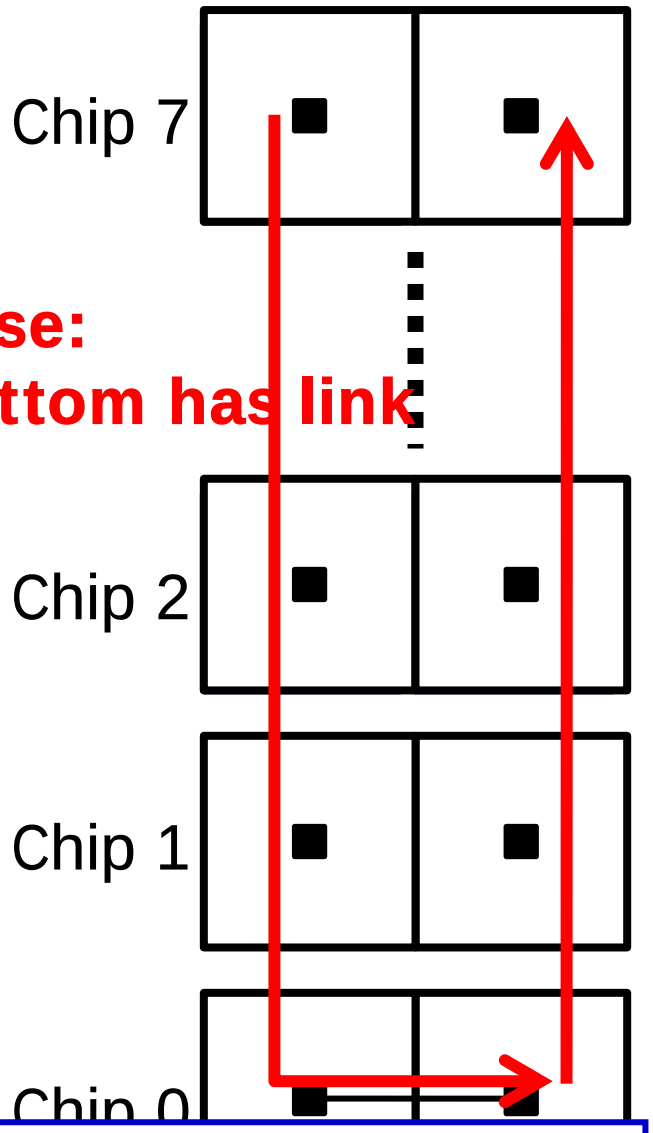


Extreme case: only the bottom has link

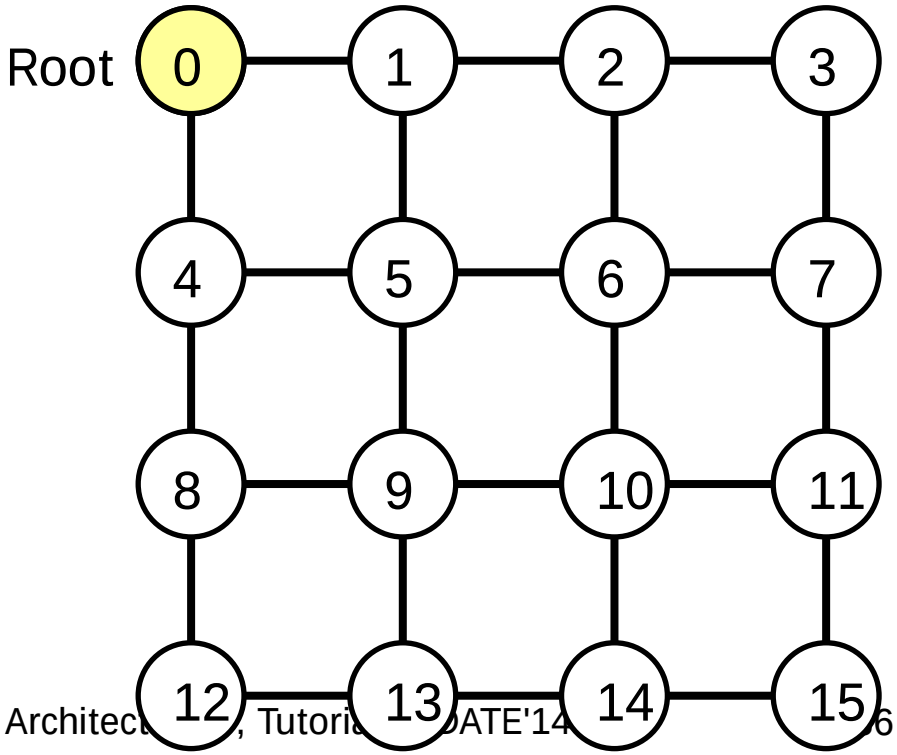
We need a mechanism to route packets even with such cases

Irregular approach: Up*/down* routing

- Up*/down* (UD) routing [Schroeder, JSAC'91]
  - Irregular network routing
  - A root node is selected
  - Packets go up and then go down

Note: Please refer to Part II for routing strategy for irregular WiNoCs.

- An example
  - 4x4 2D mesh
  - A root node is selected



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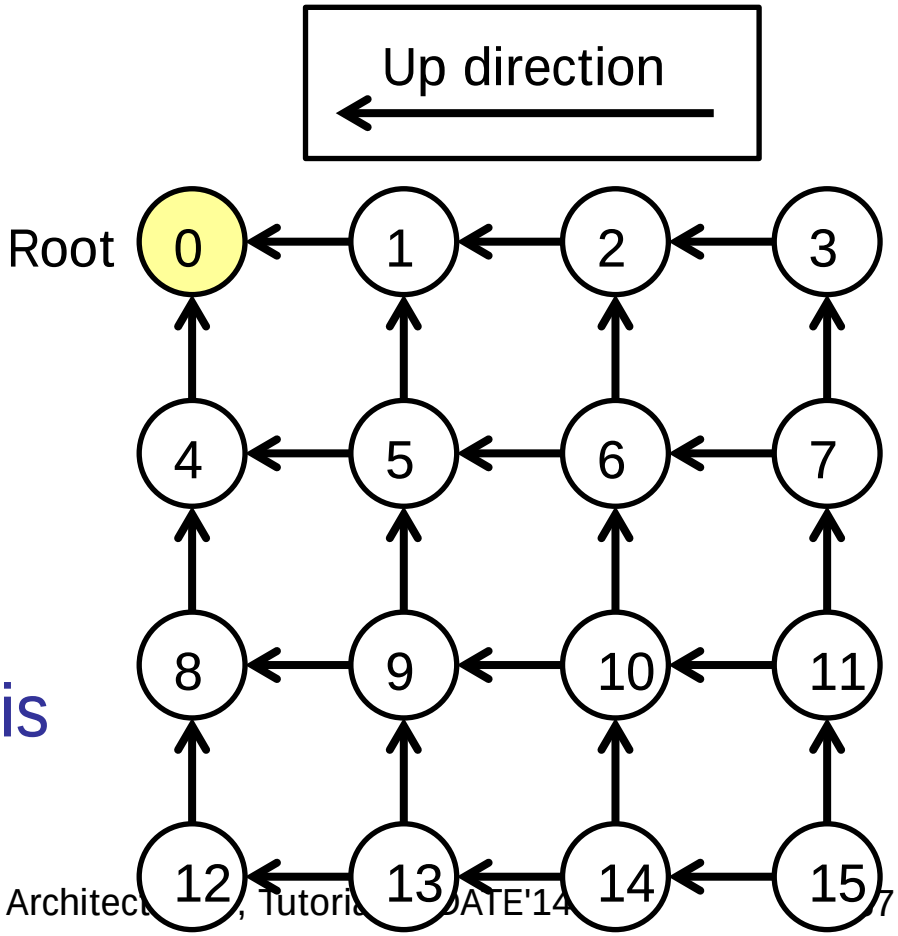
- An example
  - 4x4 2D mesh
  - Direction (up or down) is determined



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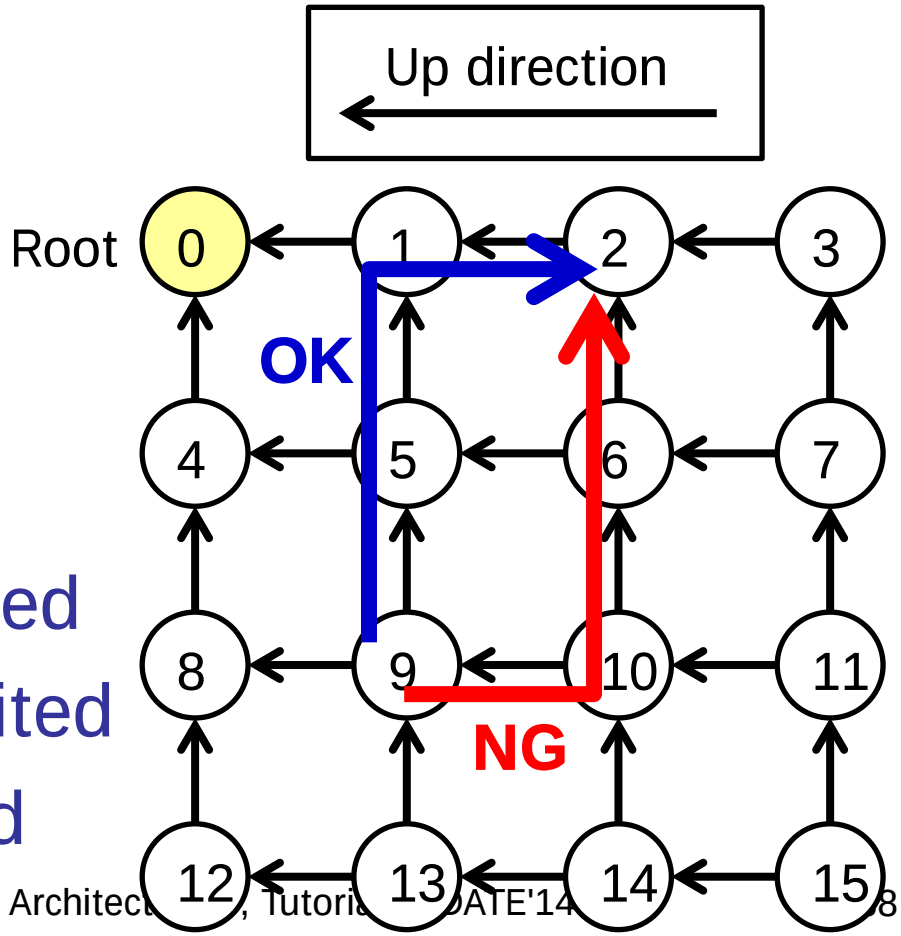
- An example
  - 4x4 2D mesh
  - Routing path is generated
  - Down-up turn is prohibited
  - It generates imbalanced paths



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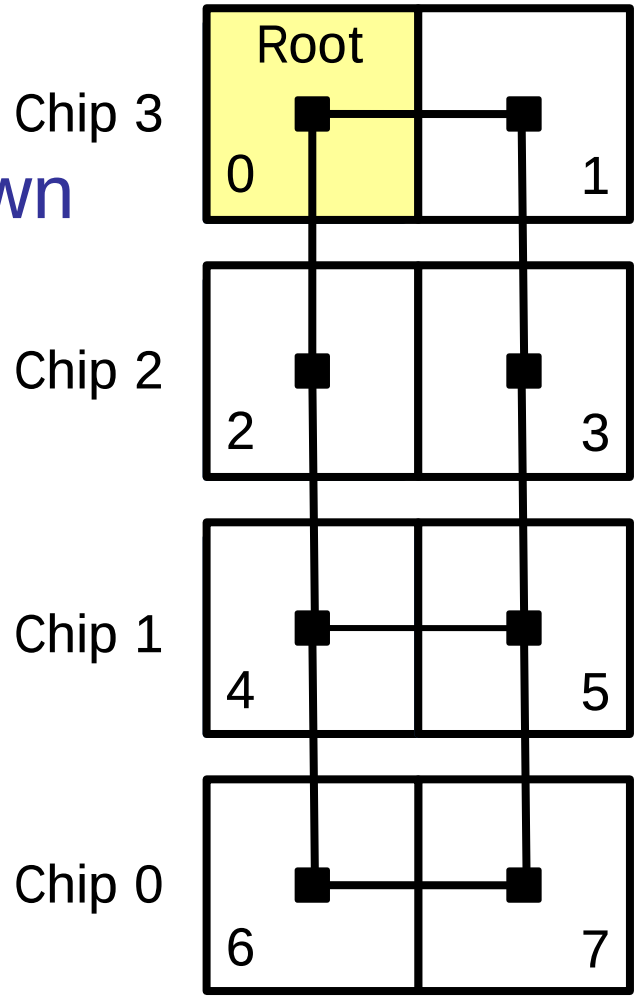
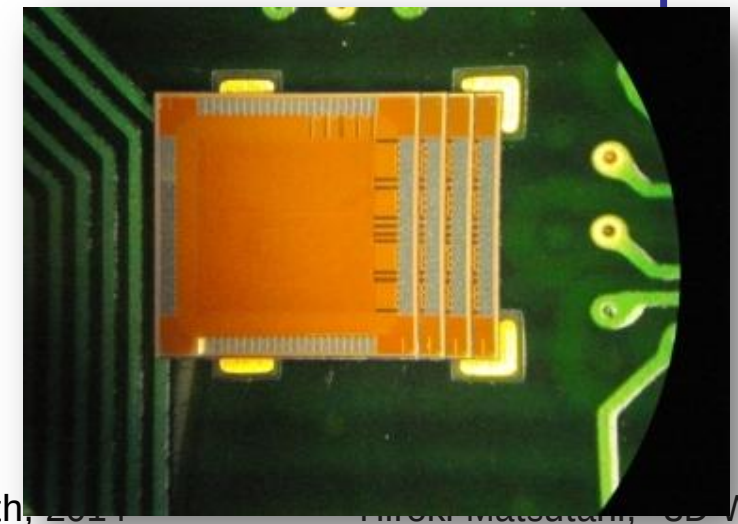


- Another example
  - 3D NoC with 4 chips



Irregular approach: Up*/down* routing

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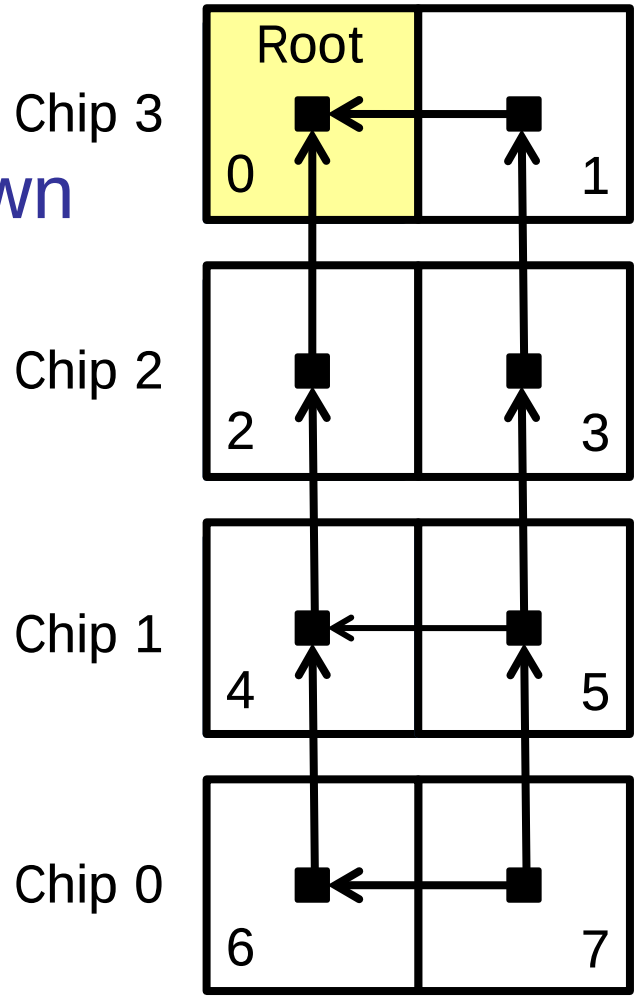

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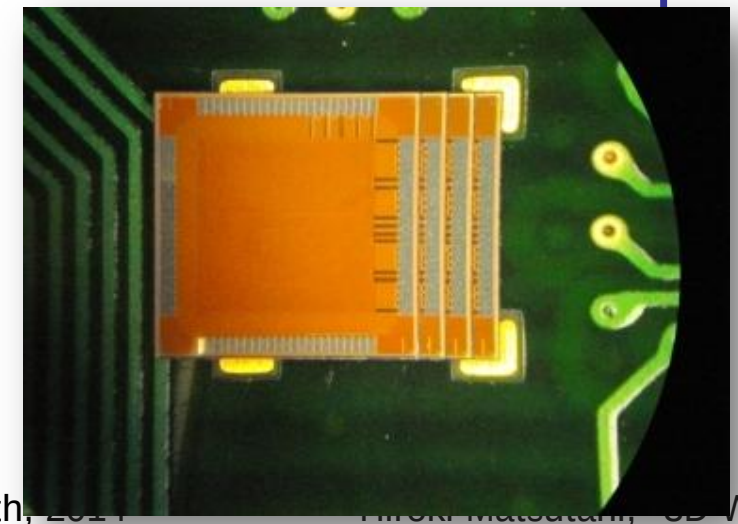

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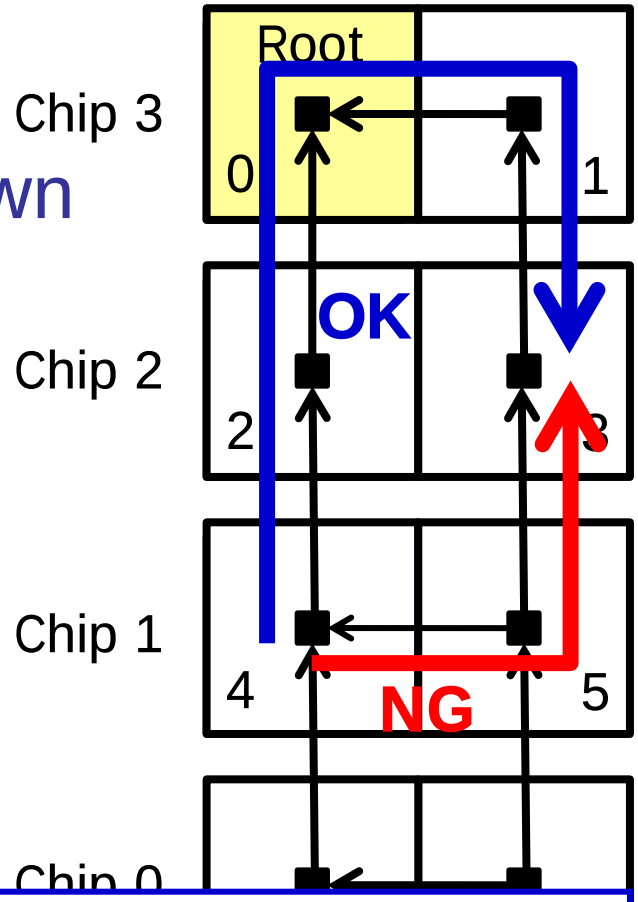

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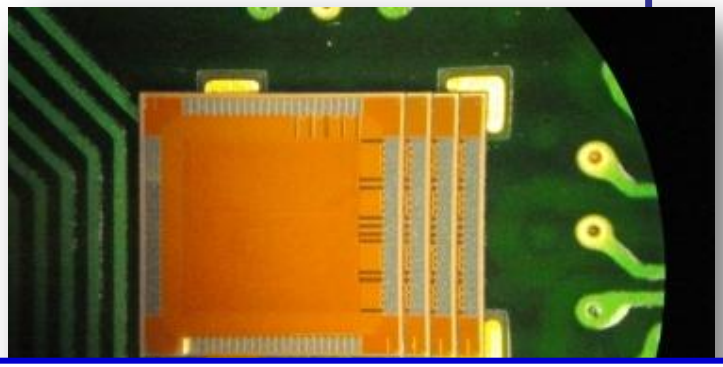
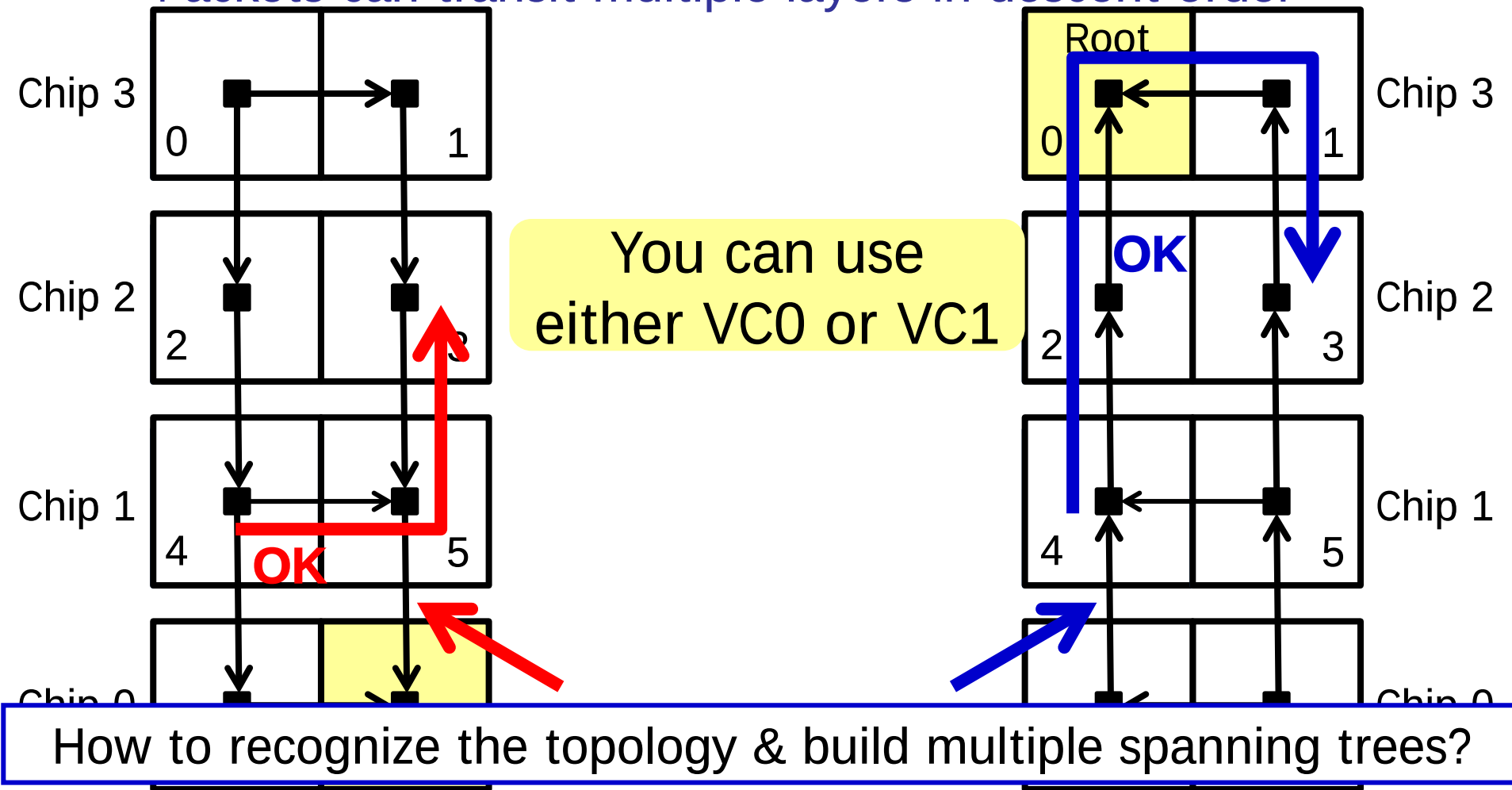


The best spanning tree root is selected by exhaustive or heuristic using communication traces (9sec for 64-tile)

Irregular approach: UD with VCs

- UD routing with multiple VCs
  - Each layer (VC) has its own spanning tree
  - Packets can transit multiple layers in descent order

[Koibuchi,ICPP'03]
[Lysne,TPDS'06]



How to recognize the topology & build multiple spanning trees?

Outline: 3D WiNoC Architectures

So far we focused on 2D WiNoC architecture and its physical link design. This part explores 3D WiNoC architectures, especially inductive-coupling 3D option.

- 3D IC technologies: Wired vs. Wireless [5min]
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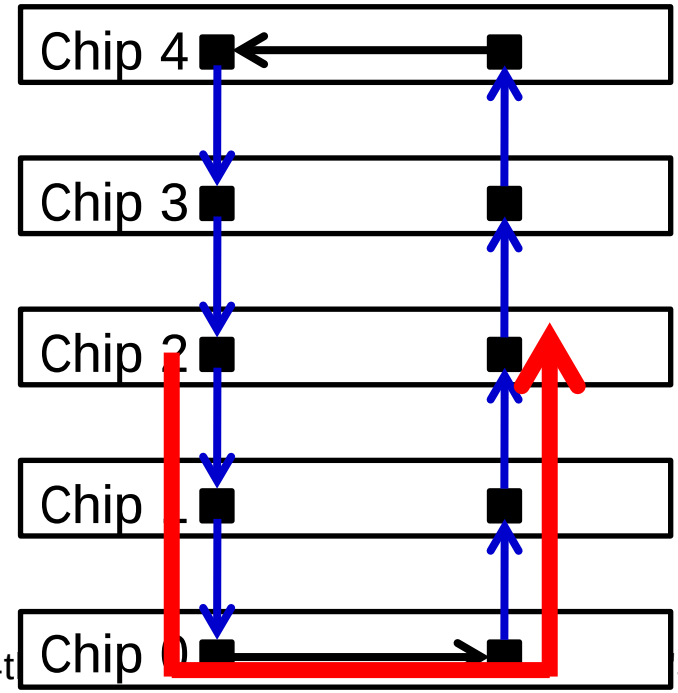
- Experiment results and Summary [10min]

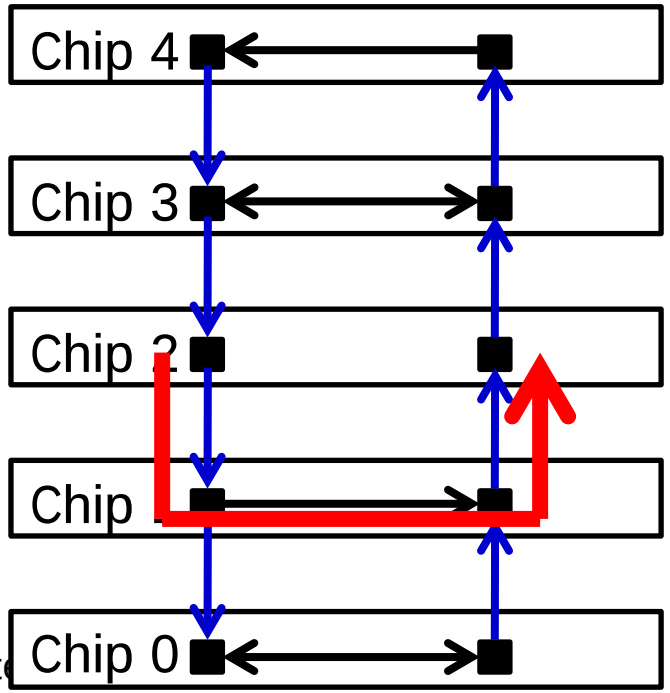
Full-system CMP simulations

Application performance of two approaches is evaluated

- Ring-based approach
  - Good Easy to add & remove
  - Bad – Inefficient hop count
  - Bad – No scalability
- Irregular approach
  - Good We can use any links
  - – Irregular routing needed
  - – Plug-and-play protocol

[Matsutani, NOCS'11]

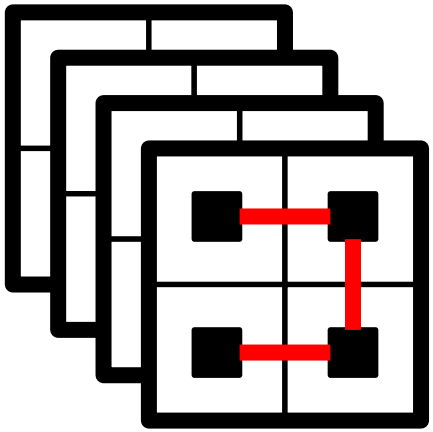




Network topology: Irregular

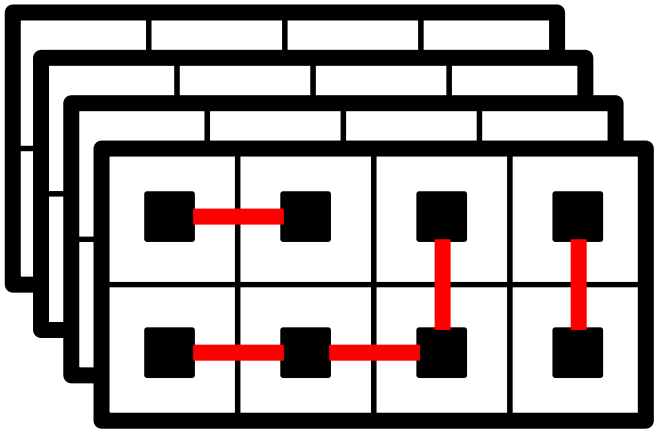
- The following iteration is performed 1,000 times
  - Each tile has router and core (e.g., processor or caches)
  - Each horizontal link appears with 50%
- We examined three cases: 16, 32, and 64 tiles

16-tile (2,2,4)



2x2 mesh * 4chips

32-tile (4,2,4)



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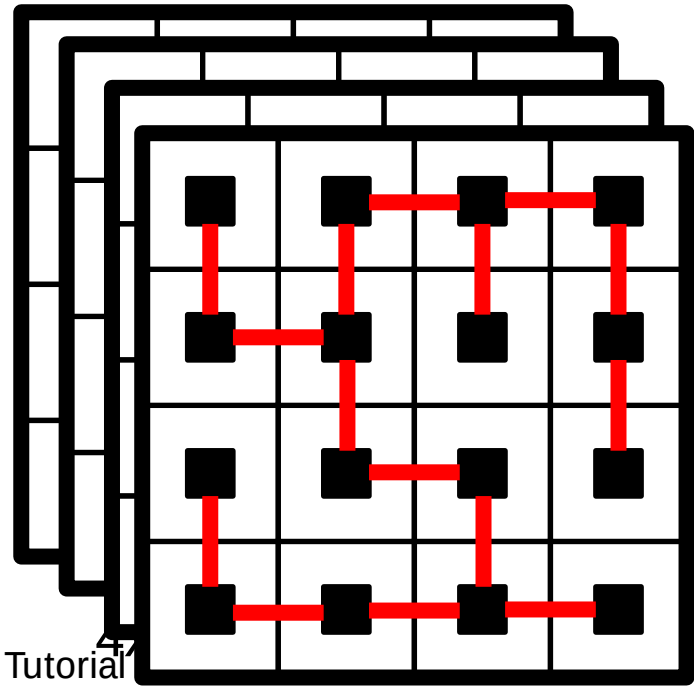
64-tile (4,4,4)



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Among 1,000 random topologies, one with the most typical hop count value is selected for the full-system evaluation

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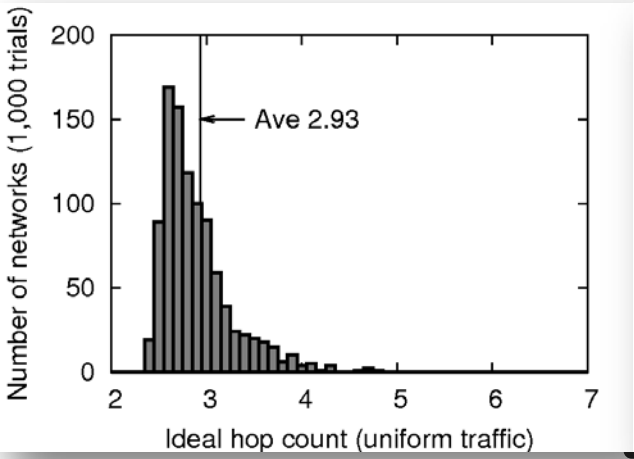

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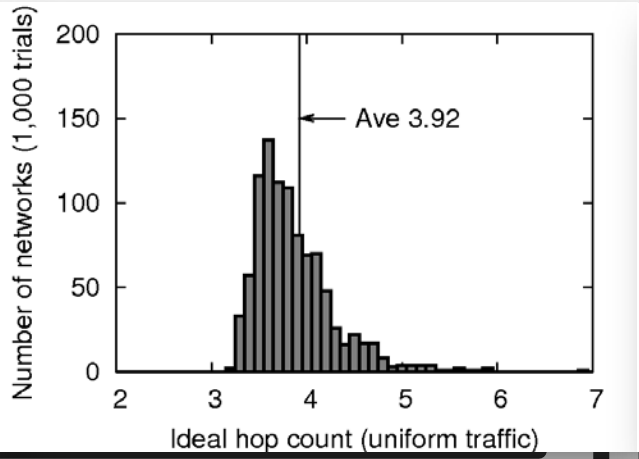

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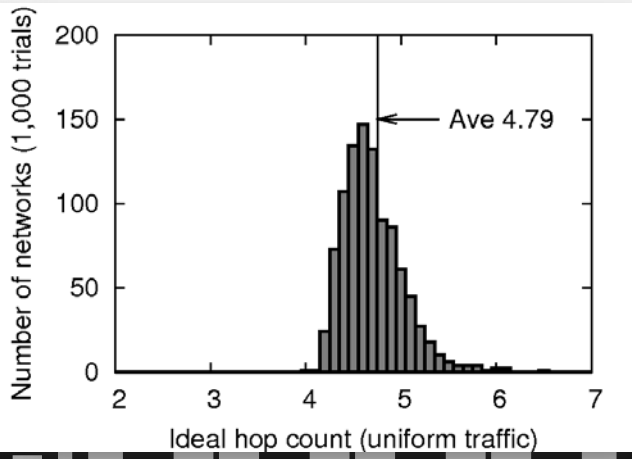

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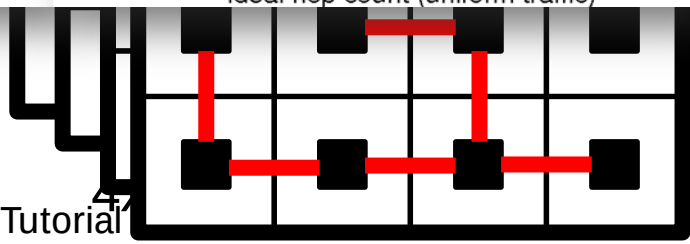

Parallel programs are running on it

GEMS/Simics is used for full-system simulations

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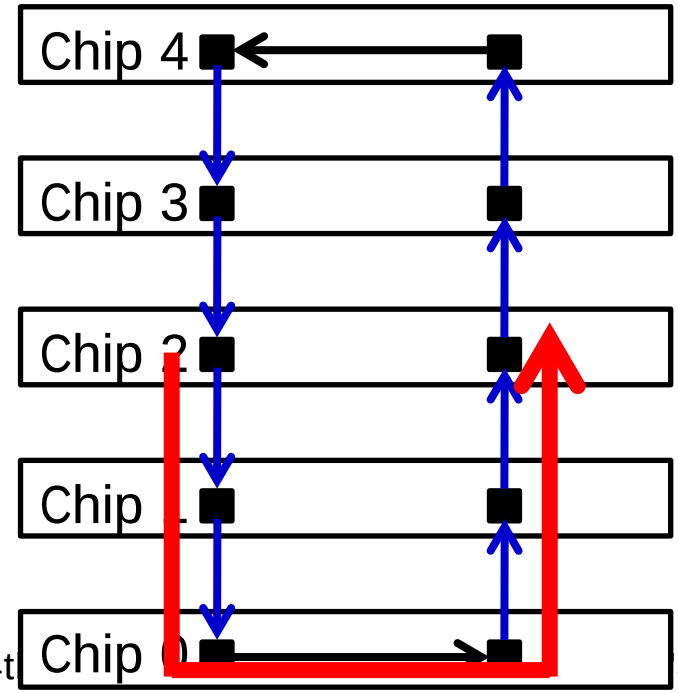
[Matsutani, NOCS'11]



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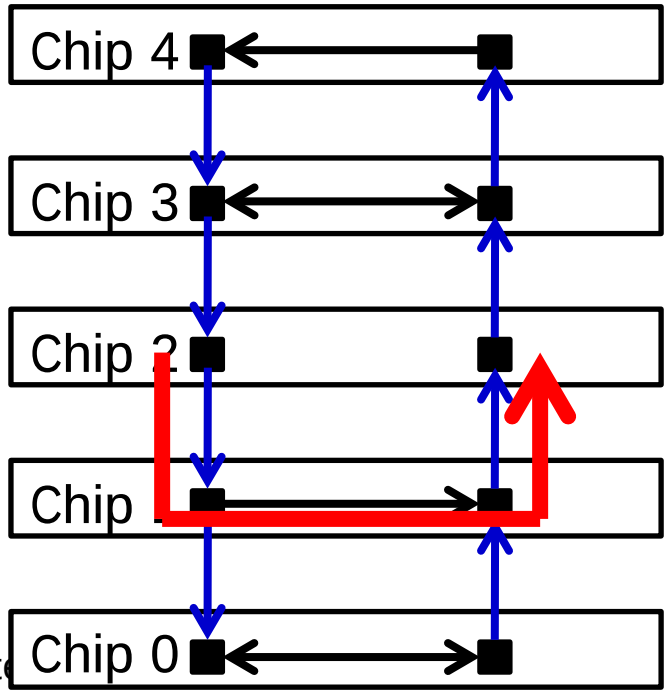
[Matsutani, ASPDAC'13]



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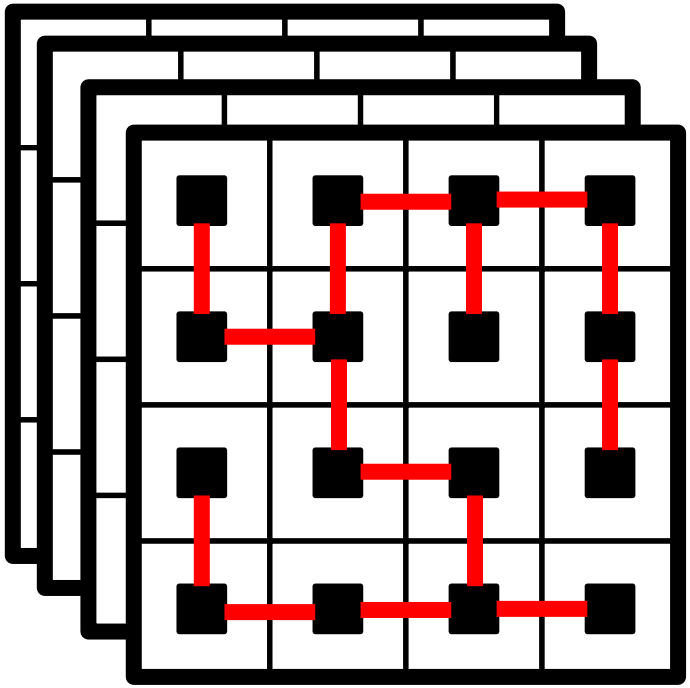


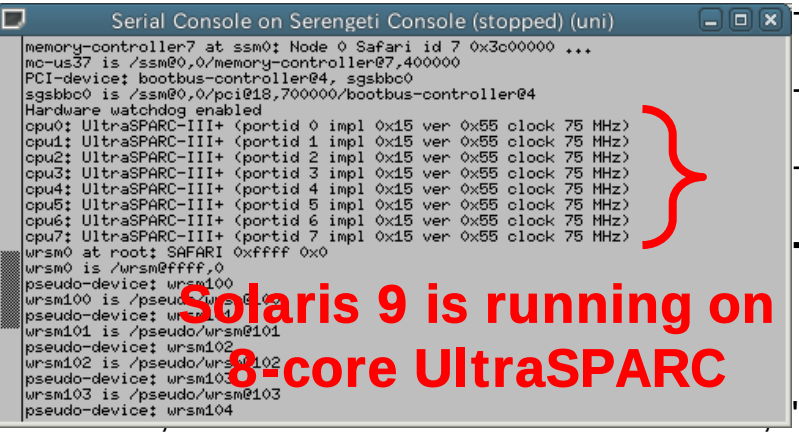


Table 1: Topologies to be examined

	Routers	CPUs	L2$banks	MCs
16-tile	16	4	32	4
32-tile	32	8	64	8
64-tile	64	8	128	16

Table 2: Simulation parameters

L1$ size & latency	64K / 1cycle
L2$ size & latency	256K / 6cycle
Memory size & latency	4G / 160cycle
Router latency	[RC/VSA] [ST] [LT]
Router buffer size	5-flit per VC
Protocol	MOESI directory

Table 3: Application programs

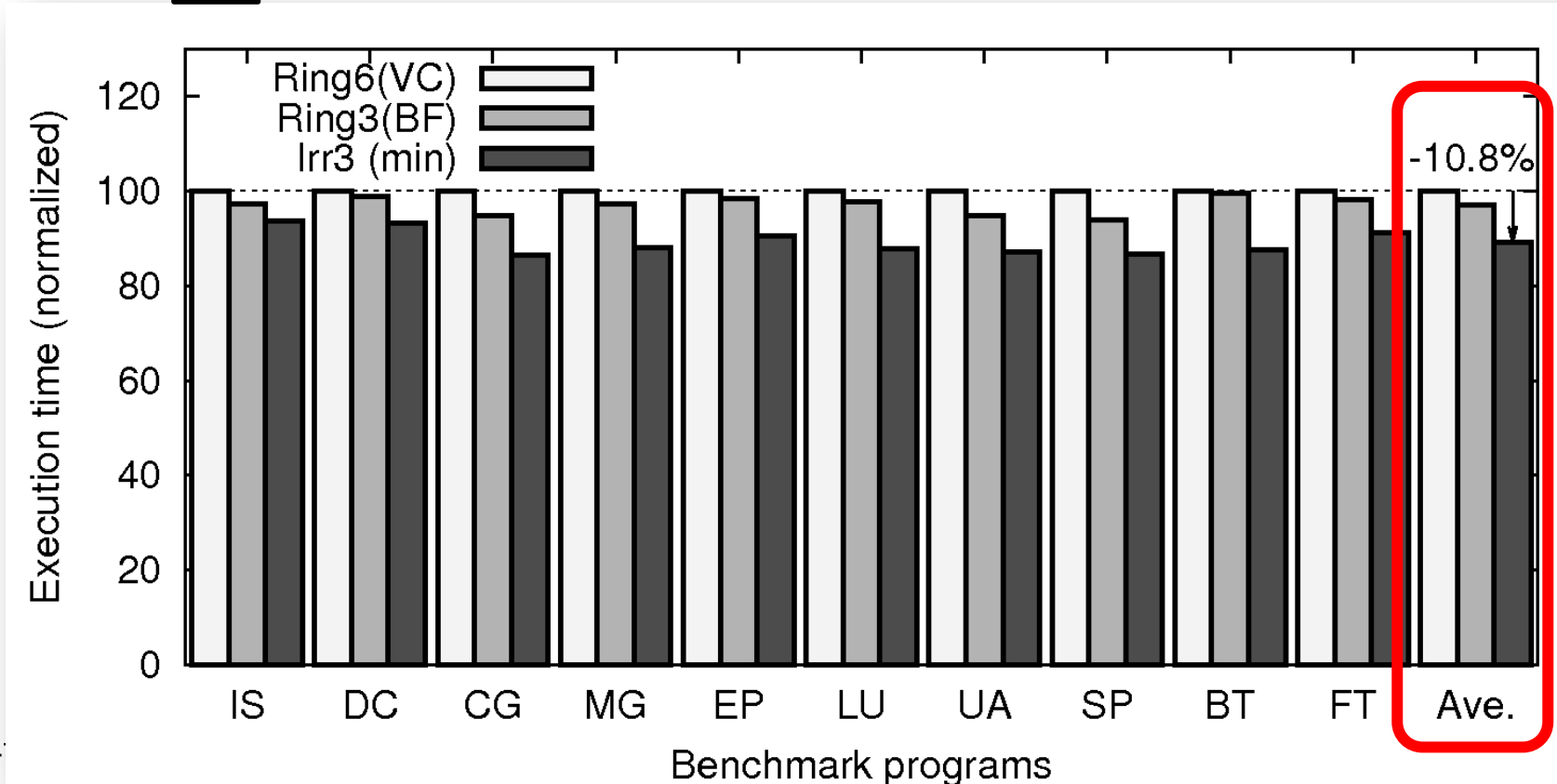
NPB (IS, DC, CG, MG, EP, LU, UA, SP, BT, FT)

Application exec time: 16-tile

Ring-based approach (VC flow & Bubble flow controls)

Irregular approach

- Irregular approach outperforms Ring-based one by 10.8% in 16-tile case.

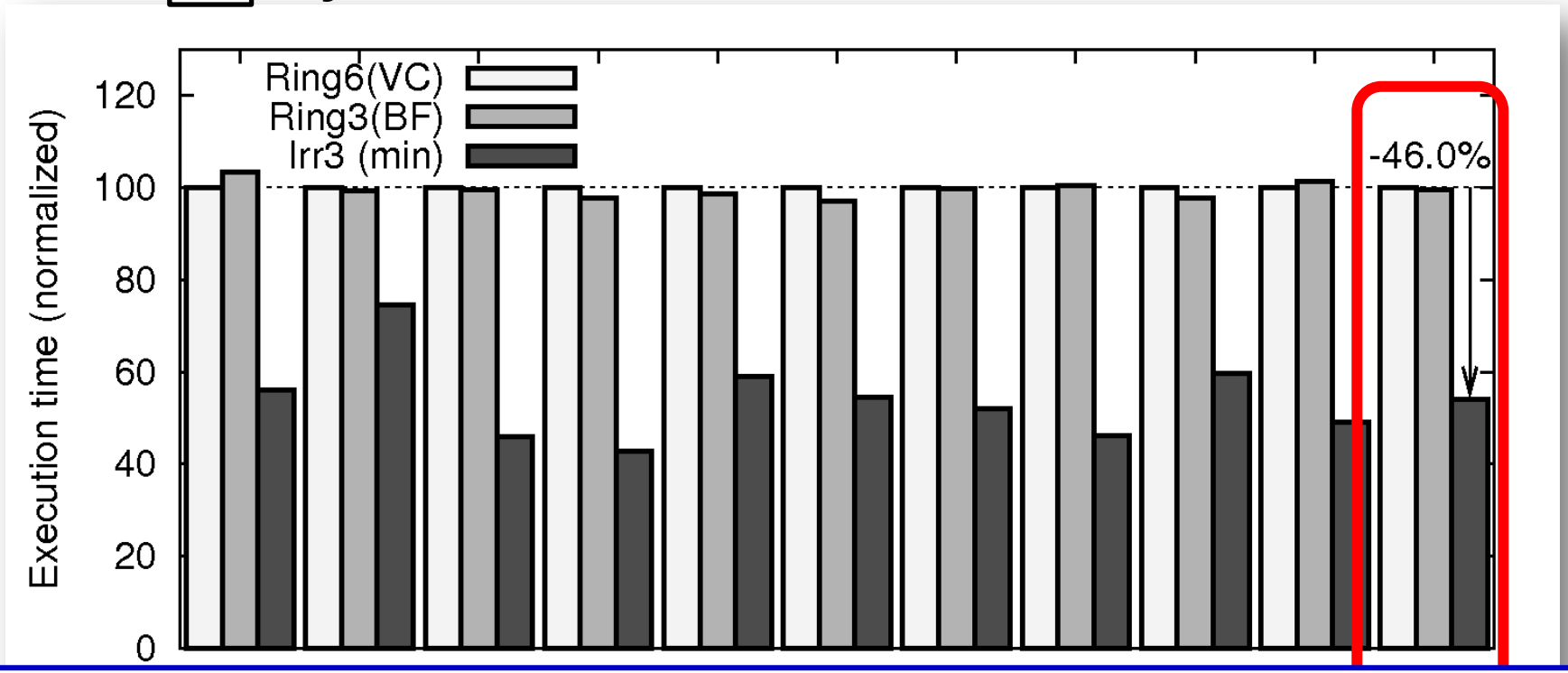


Application exec time: 64-tile

Ring-based approach (VC flow & Bubble flow controls)

Irregular approach

- Irregular approach outperforms Ring-based one by 46.0% in 64-tile case.



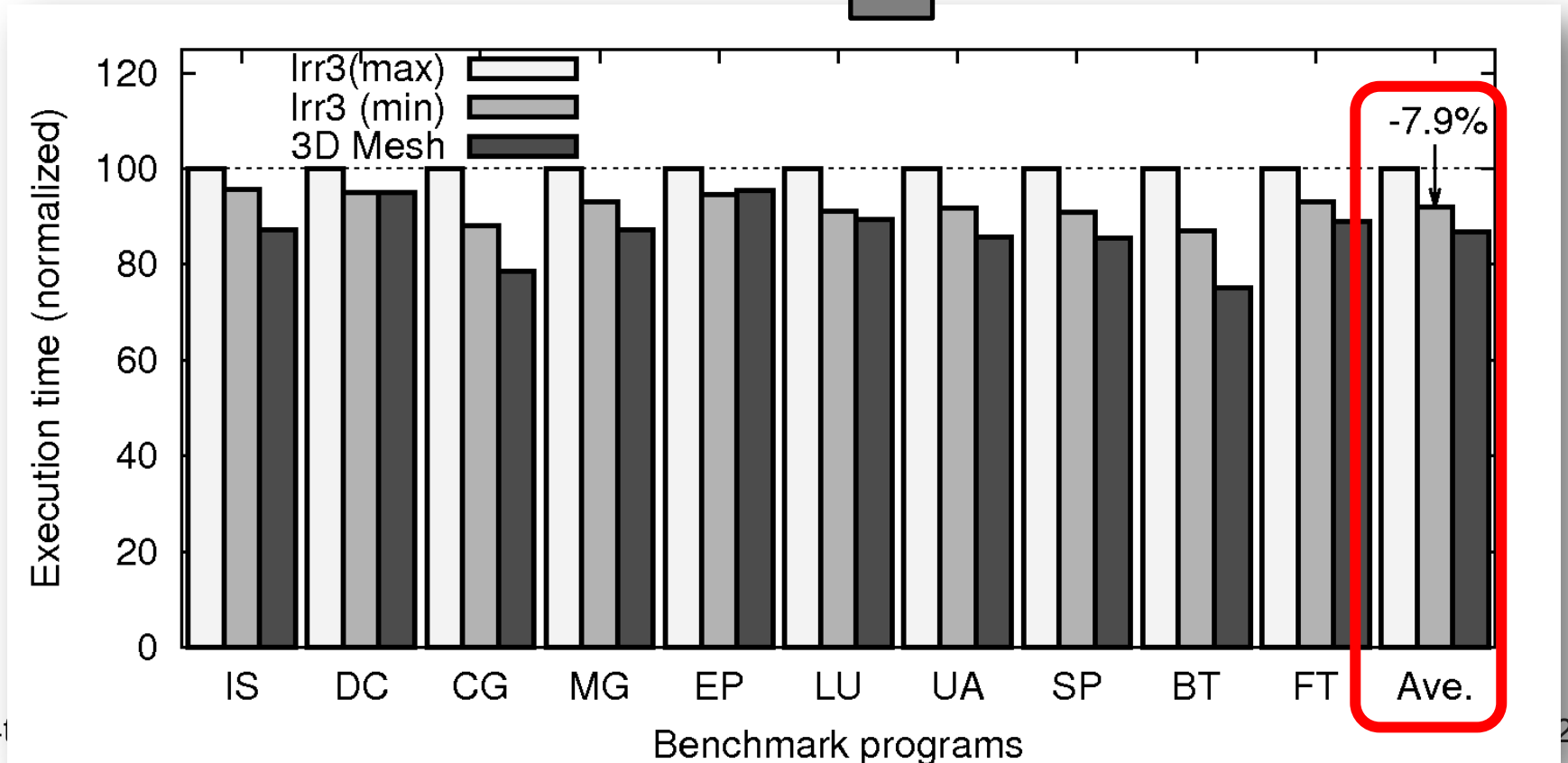
Ring has no scalability → Irregular one improves significantly

Application exec time: 16-tile

Irregular (**50% of horizontal links are implemented**)

3D mesh (**all horizontal links are implemented**)

- Performance of Irregular approach Irr3(min) is closed to that of 3D mesh



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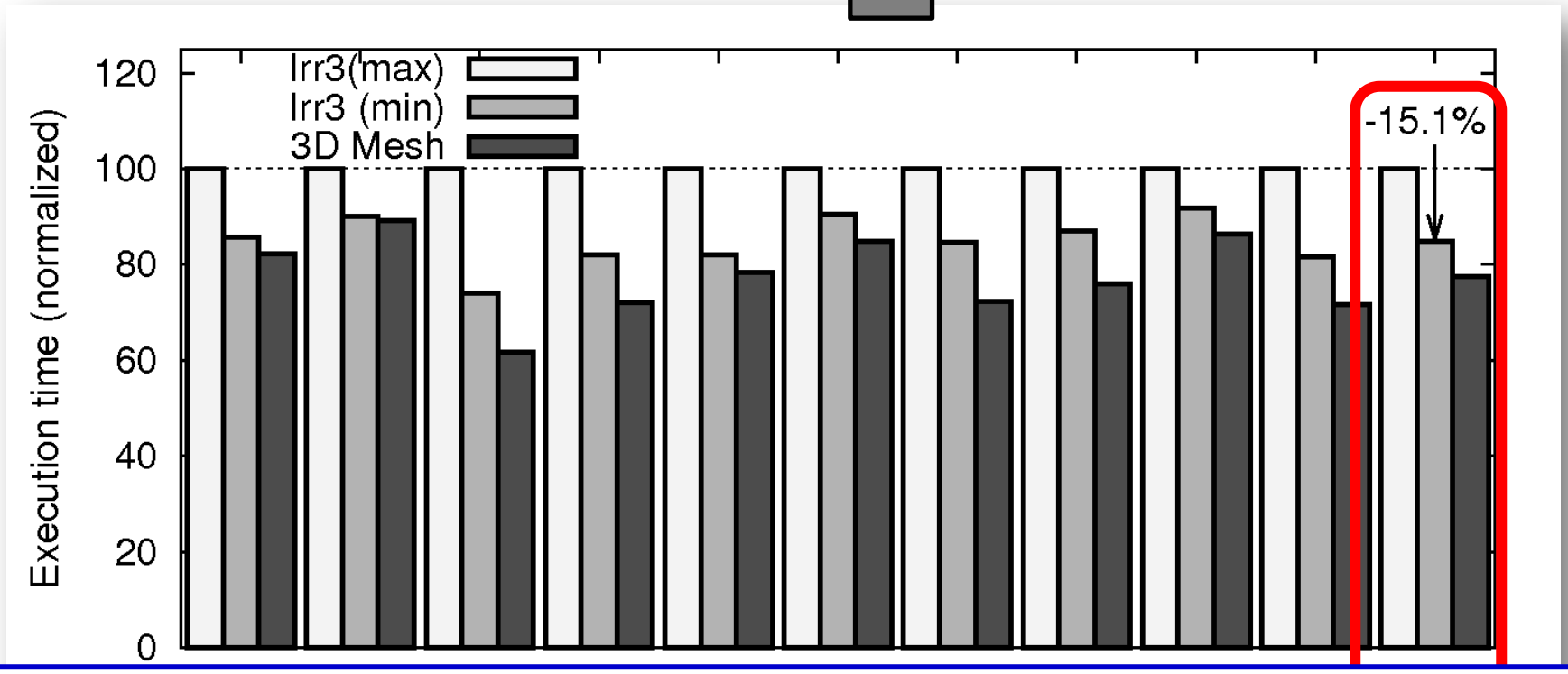
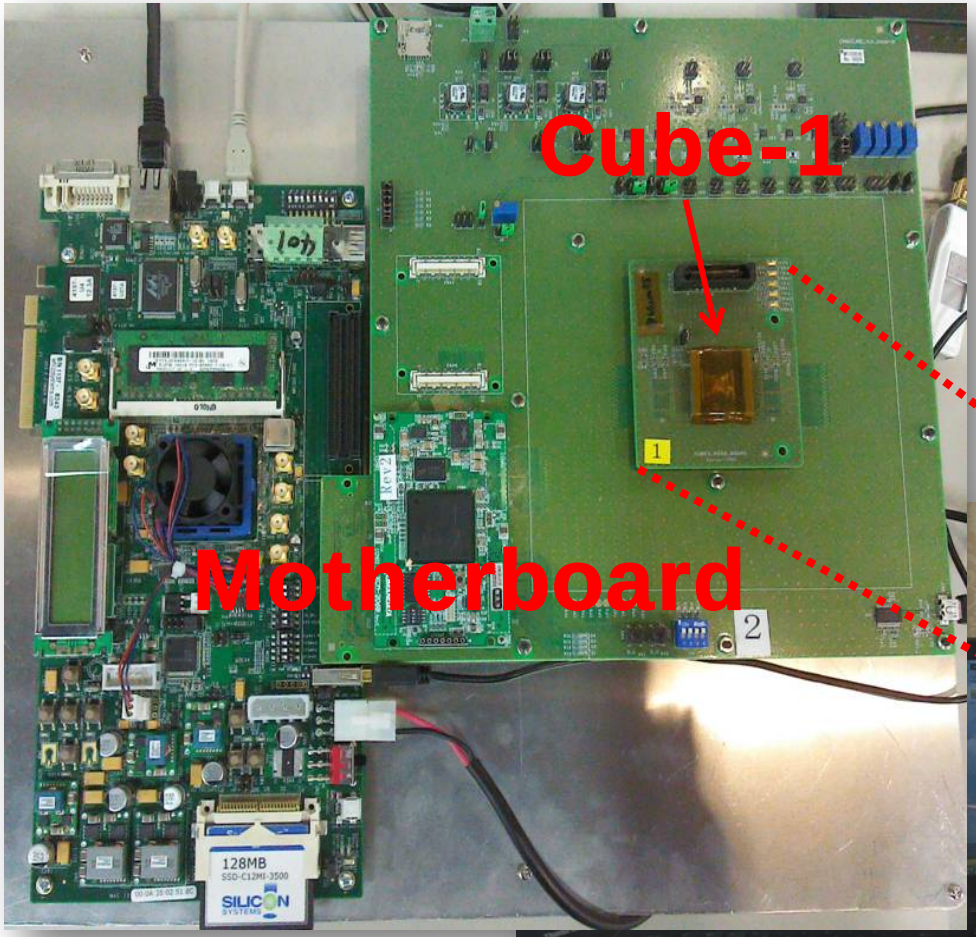


Optimized Irr3(min) improves by 15.1% compared to the worst

Experiment results: Cube-1 (2012)

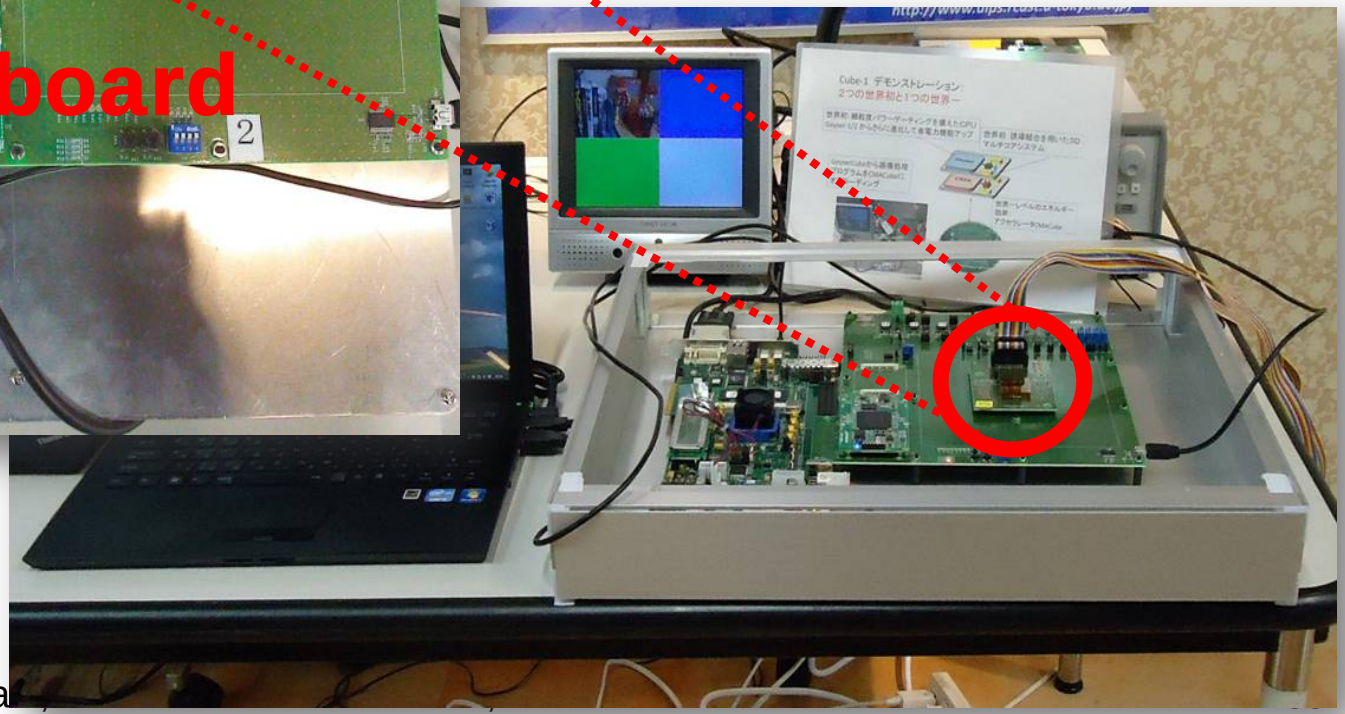


Cube-1 demo system

PE array chip performs image processing

CPU chip for control

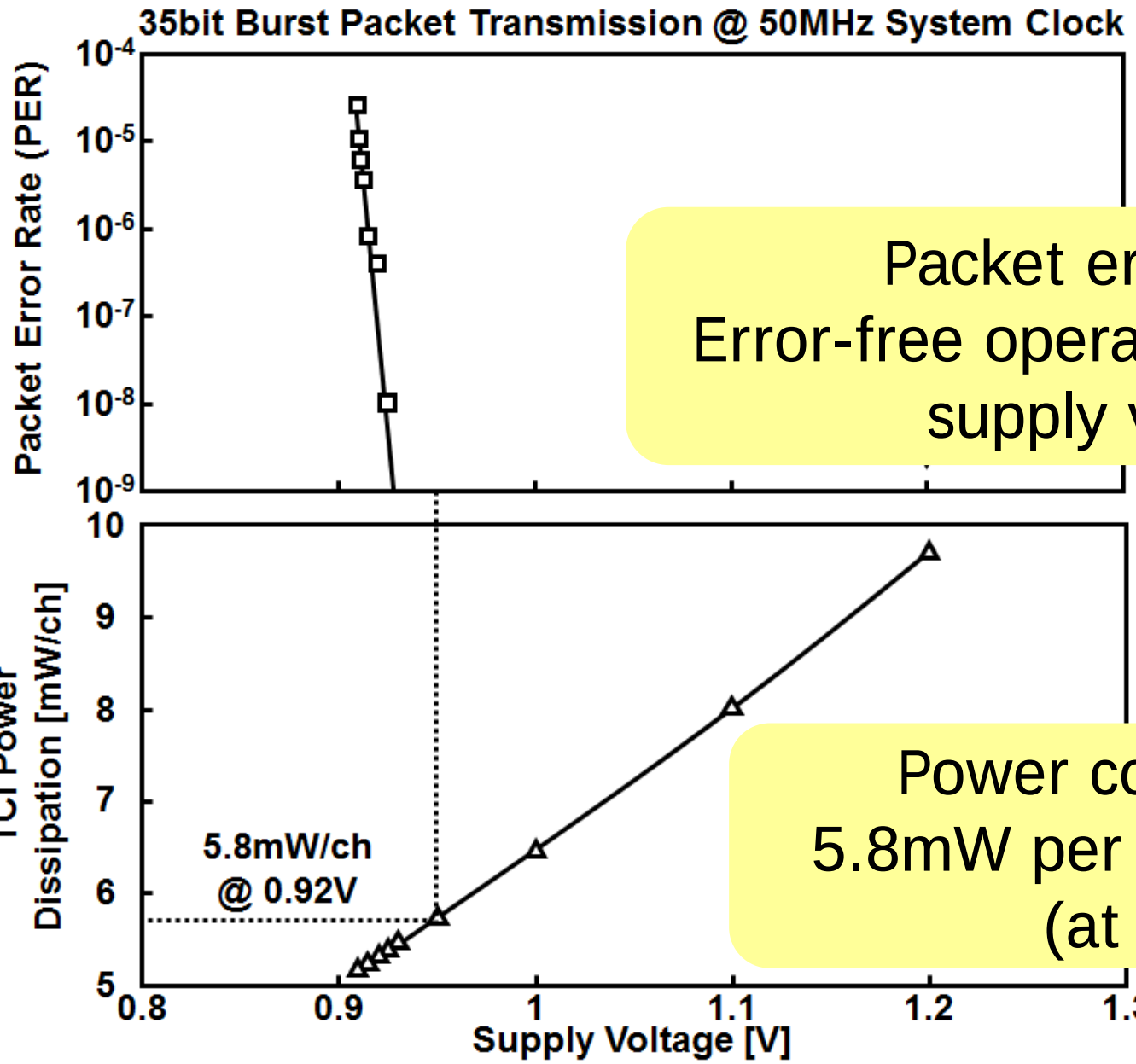
[Miura, HotChips'13 Demo]



Experiment results: Cube-1 (2012)

Process	Technology	65nm CMOS (12-Metal)
	Chip Area	2.1mm x 4.2mm
	Core Area	1.5mm x 3.6mm
Host CPU	CPU Core	MIPS R3000 Compatible
	Cache	4KB 2Way Instruction Cache 4KB 2Way Data Cache 16-Entry Shared TLB
	I/O	3Gb/s TCI, 100Mb/s 32bit External I/O
	Supply Voltage	Core+TCI: 1.2V External I/O: 3.3V
Accelerator	PE Array	64 (8x8) Array
	Micro-Controller	1Cycle Non-Pipelined
	Memory	25bit 2KB 2Bank Data Memory 14bit 128depth Instruction Memory
	I/O	3Gb/s TCI x 2Channels for Up/Downlinks
	Supply Voltage	PE Array: 0.5~1.2V DVS Other Core+TCI: 1.2V
3D Processor	System Clock	50~100MHz
	Chip Stack	Staircase Stacking Host CPU+Accelerator x1 Stack Host CPU+Accelerator x3 Stack
	Chip Thickness	40μm (Bottom Chip: 300μm)

Experiment results: Cube-1 (2012)



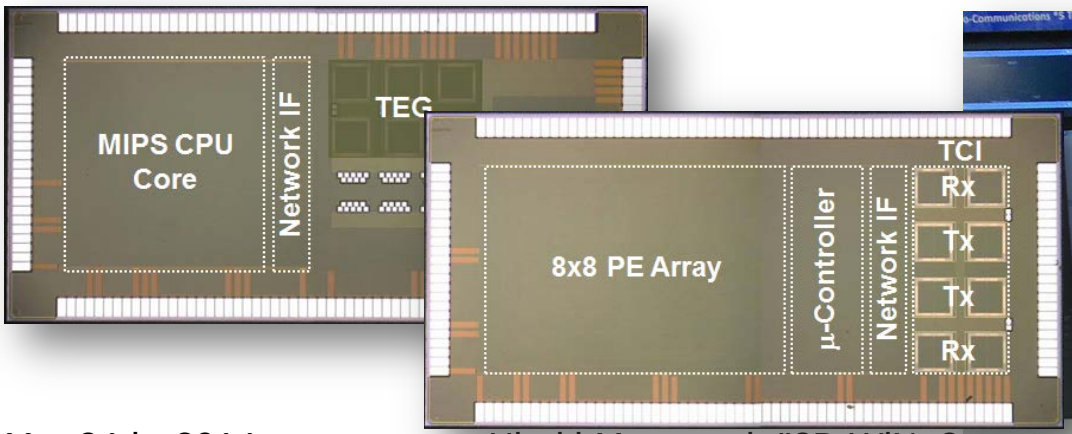
[Miura, IEEE Micro 13]

Packet error rate:
Error-free operation at nominal supply voltage

Power consumption:
5.8mW per 2Gbps channel
(at 0.92V)

Summary: 3D WiNoC Architectures

- Inductive-coupling 3D SiP
  - A low cost alternative to build low-volume custom systems by stacking off-the-shelf known-good-dies
  - No special process technology is required; inductors are implemented with metal layers
- Cube-1: A practical 3D WiNoC system
  - Two types: Host CPU chip & Accelerator chips
  - We can customize number & types of chips in SiP



Future plans: 3D WiNoC Architectures

Cube-2 design:

- STM 28nm process
- CPU & Accelerator chips
- Memcached accelerator chip for smart sensors

Power/heat management:

- Dynamic on/off control of inductors
- Closed-loop control [Elfadel, DATE'13]

(See Part I)

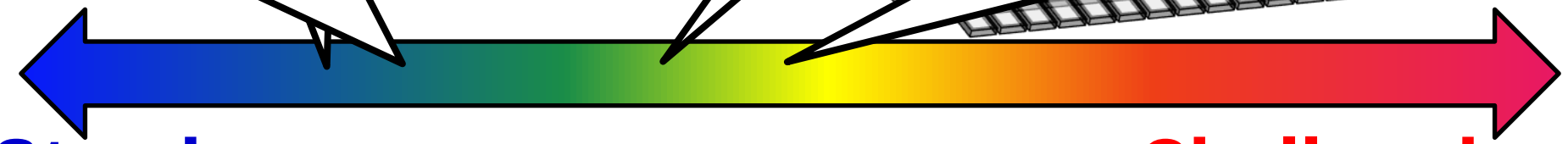
All-in-one TX/RX macro:

- Coil + Routers/buffers
- Coil uses only metal layers; silicon available

Combine 2D & 3D WiNoC:

- mm-wave wireless for intra-chip

(See Parts II and III)



Steady **Challenging**

Future plans: 3D WiNoC Architectures

Jumbo inductors:

- Jumbo inductor like a power ring
- <1mm communication
- Relax SiP assembly

Cartridge style computer:

- Insert necessary chips
- Power/clk from cartridge
- Inter-chip data transfers use wireless
- Power from wireless ??

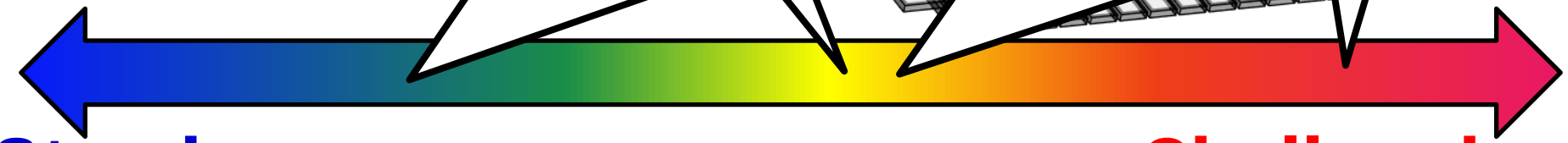
Wireless broadcast bus:

- Combine wireless vertical bus & P2P links
- Static/dynamic TDMA vs. CSMA/CD

Exploiting small-world:

- Add a random NoC chip to 3D WiNoC SiP to shorten path length

(See Part I)



Steady **Challenging**

References (1/2)

- Cube-0: The first real 3D WiNoC
  - H. Matsutani, et.al., "A Vertical Bubble Flow Network using Inductive-Coupling for 3-D CMPs", NOCS 2011.
  - Y. Take, et.al., "3D NoC with Inductive-Coupling Links for Building-Block SiPs", IEEE Trans on Computers (2014).
- Cube-1: The heterogeneous 3D WiNoC
  - N. Miura, et.al., "A Scalable 3D Heterogeneous Multicore with an Inductive ThruChip Interface", IEEE Micro (2013).
- MuCCRA-Cube: Dynamically reconfigurable processor
  - S. Saito, et.al., "MuCCRA-Cube: a 3D Dynamically Reconfigurable Processor with Inductive-Coupling Link", FPL 2009.

References (2/2)

- Vertical bubble flow control on Cube-0
  - H. Matsutani, et.al., "A Vertical Bubble Flow Network using Inductive-Coupling for 3-D CMPs", NOCS 2011.
  - Y. Take, et.al., "3D NoC with Inductive-Coupling Links for Building-Block SiPs", IEEE Trans on Computers (2014).
- Spanning trees optimization for 3D WiNoCs
  - H. Matsutani, et.al., "A Case for Wireless 3D NoCs for CMPs", ASP-DAC 2013 (Best Paper Award).