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A Building Block 3D System with Inductive-Coupling Through Chip Interfaces

Hiroki Matsutani
Keio University, Japan

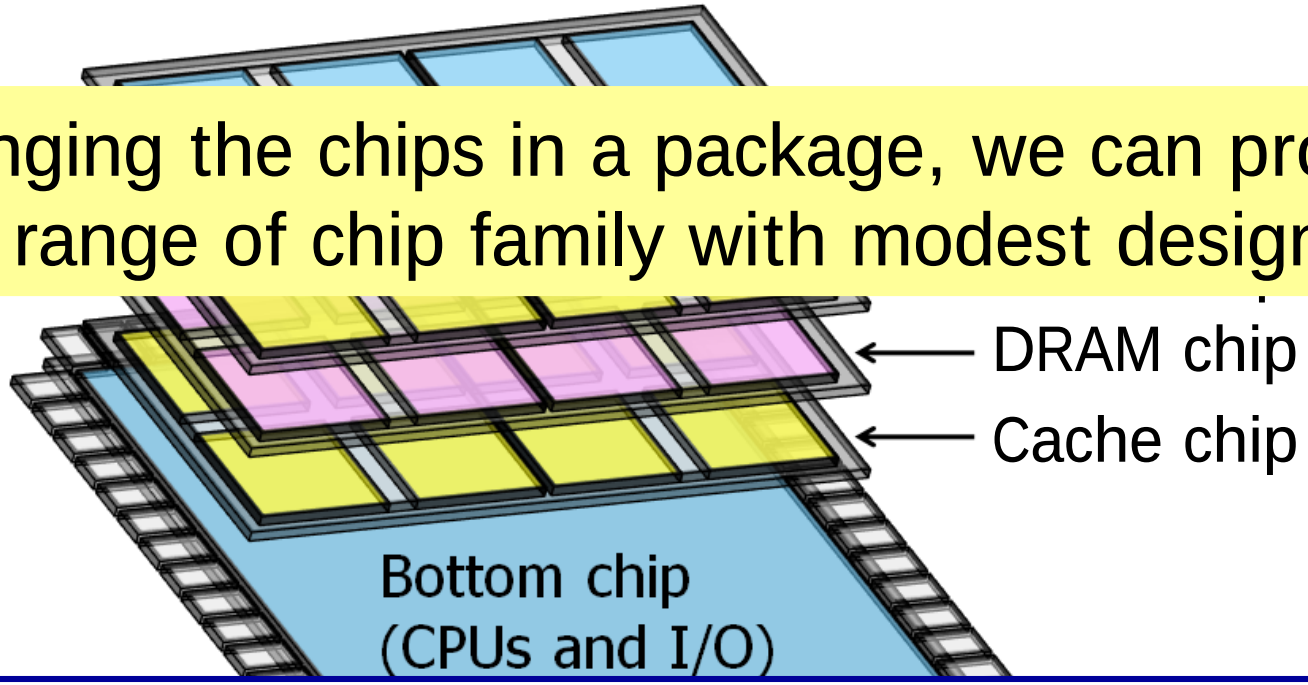
Outline: 3D Wireless NoC Designs

This part also explores 3D NoC architecture with inductive-coupling wireless links and shows some prototype designs

- 3D IC technologies: Wired vs. Wireless [5min]
- Prototype systems: Cube-0 & Cube-1 [5min]
  - 3D Ring network
- Prototype system: Cube-2 [5min]
  - 3D Linear network
- Summary and Q&A [5min]

Design cost of LSI is increasing

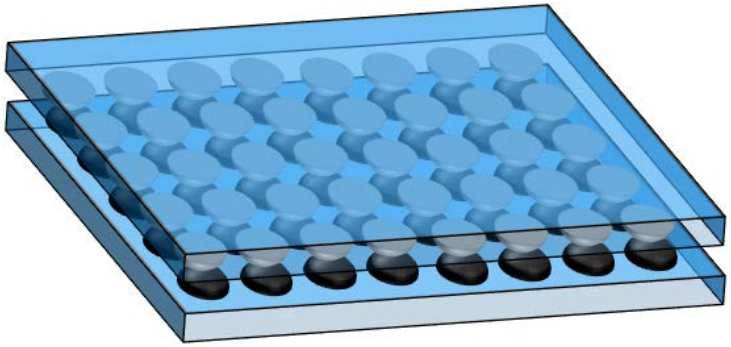
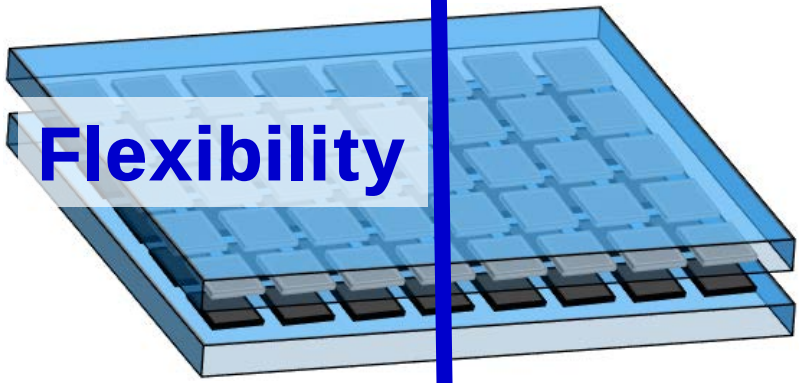
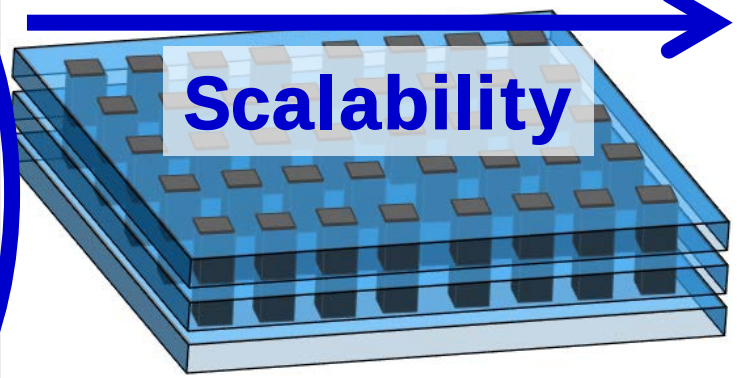
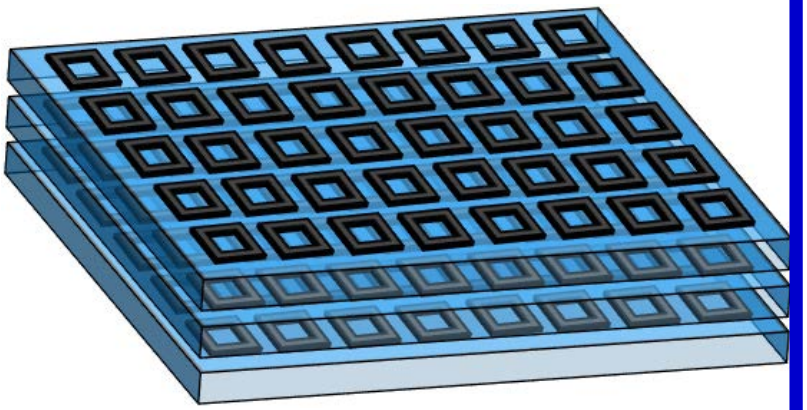
- System-on-Chip (SoC)
  - Required components are integrated on a single chip
  - Different LSI must be developed for each application
- System-in-Package (SiP) or 3D IC
  - Required components are stacked for each application



By changing the chips in a package, we can provide a wider range of chip family with modest design cost

Next slides show techniques for stacking multiple chips

3D IC technology for going vertical

	Wired	Wireless
Two chips (face-to-face)	 Microbump	 Capacitive coupling
More than three chips	 Through silicon via	 Inductive coupling

Flexibility

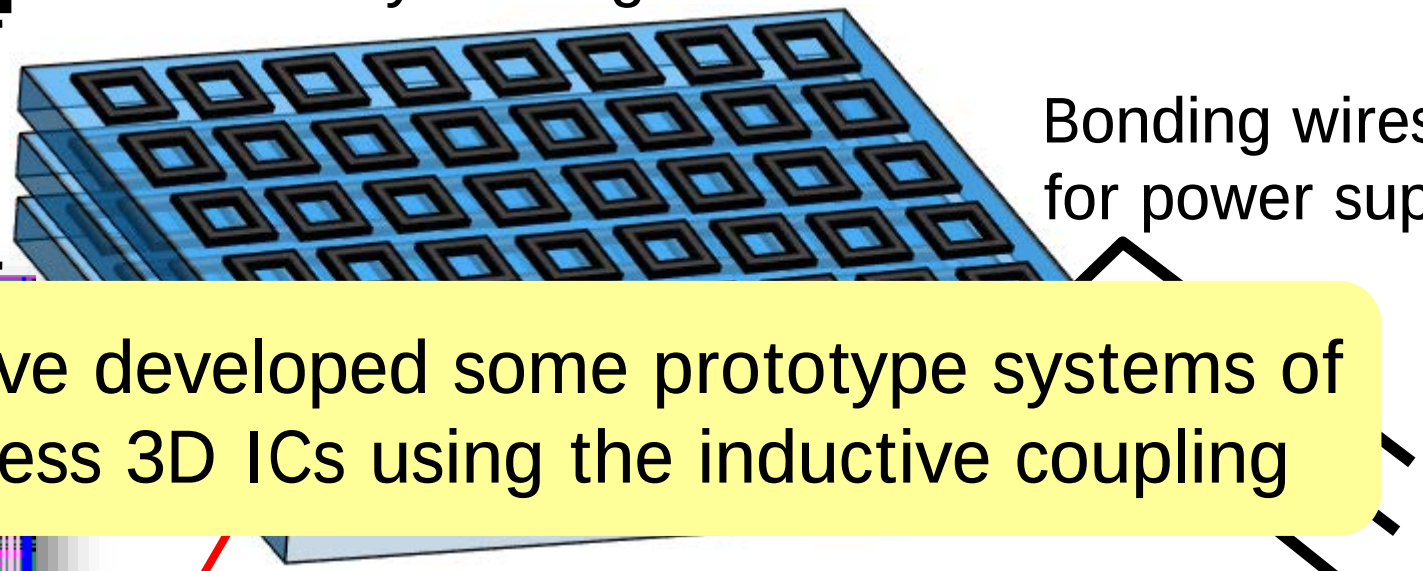
Scalability

Inductive coupling link for 3D ICs

Stacking after chip fabrication

Only know-good-dies selected

More than 3 chips



Bonding wires for power supply

We have developed some prototype systems of wireless 3D ICs using the inductive coupling

Inductor for transceiver

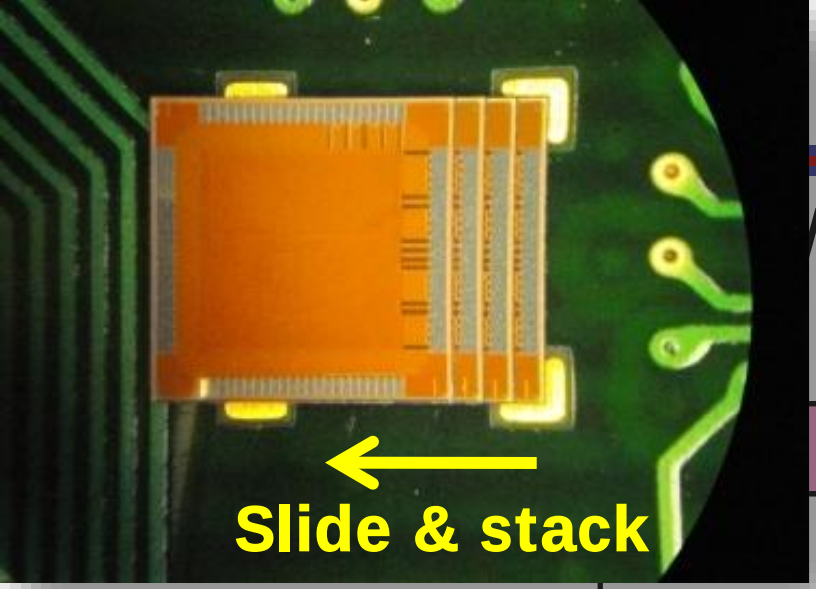
Implemented as a square coil with metal in common CMOS

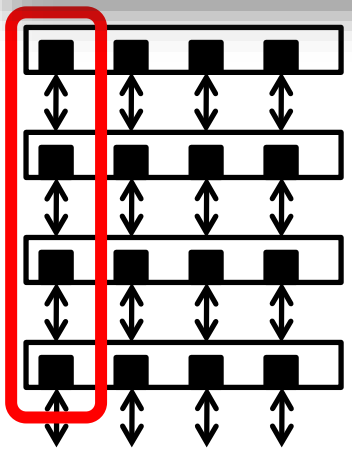
Footprint of inductor

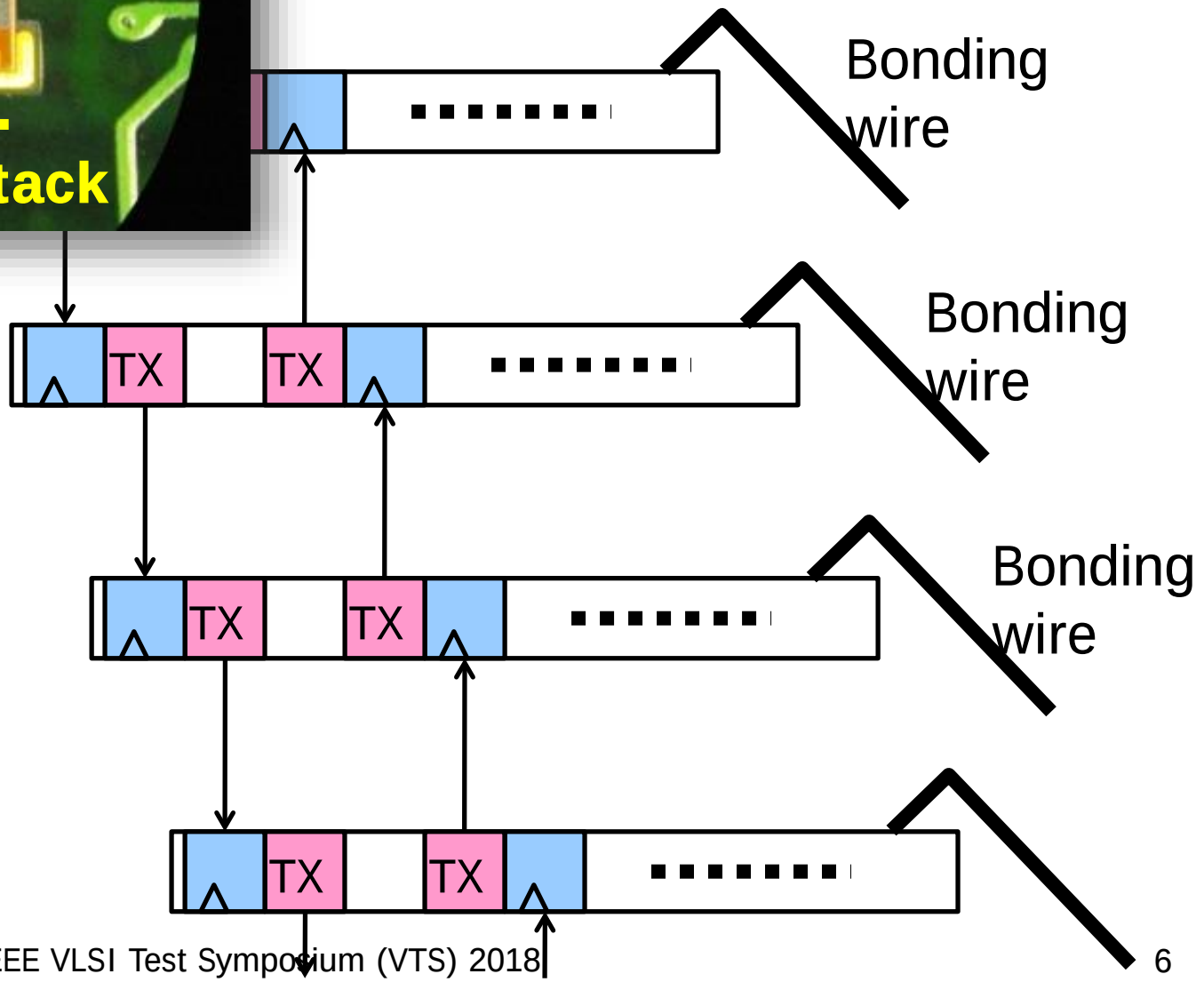
Not a serious problem. Only metal layers are occupied

hod: Staircase stacking

Idle modes (mode change 1-cycle)







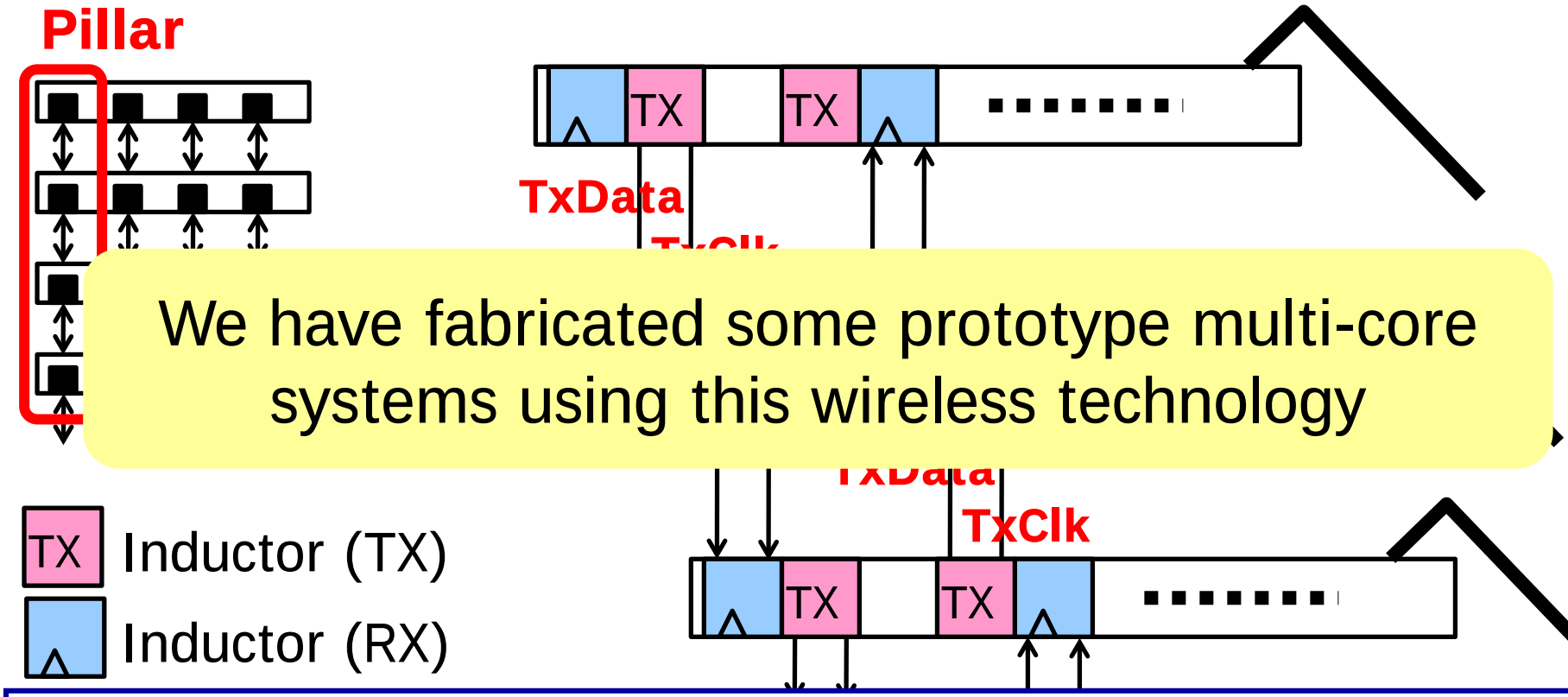
TX Inductor (TX)

Inductor (RX)

Stacking method: Staircase stacking

- Inductive-coupling link
  - Local clock @ 4GHz
  - Serial data

System clock for NoC: 200MHz
→ 35-bit transfer for each clock



We have fabricated some prototype multi-core systems using this wireless technology

Local clock shared by neighboring chips; No global sync.

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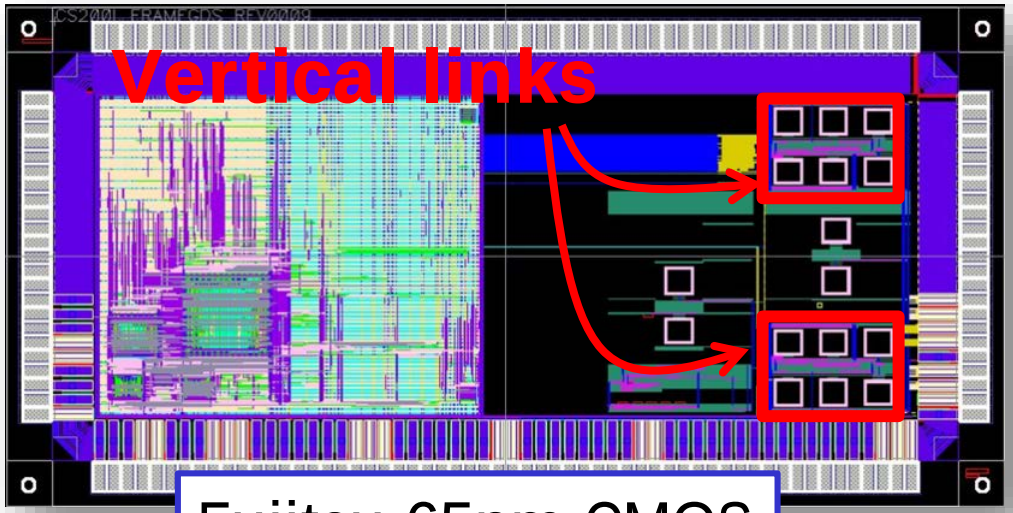
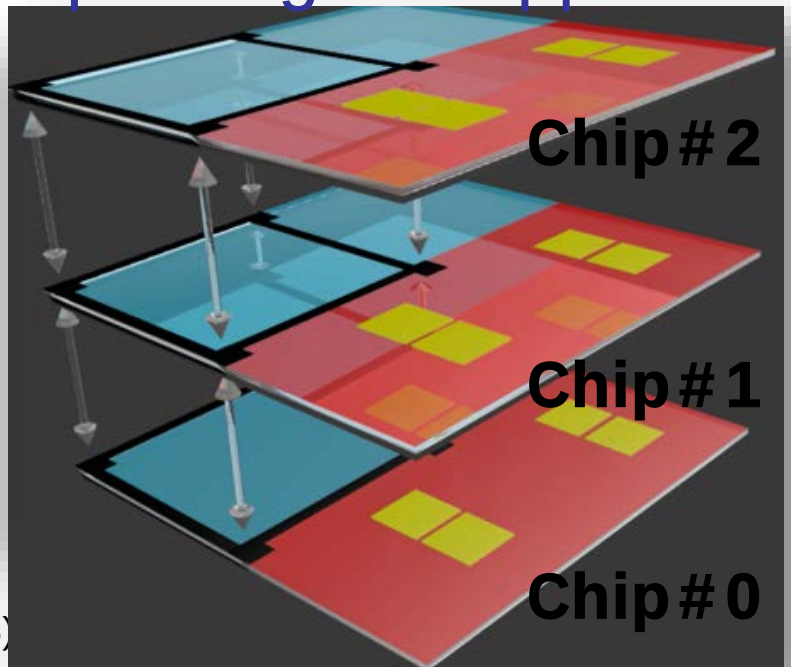
Wireless 3D chip stacking for IoT

- System-in-Package (SiP) for IoT devices
  - Required chips are selected and stacked in package
  - E.g., CPU chip, Accelerator chip, Memory chip, ...
- Wireless inductive-coupling for vertical links
  - Not electrically-connected
  - Add, remove, and swap chips for given applications



Fujitsu 65nm CMOS



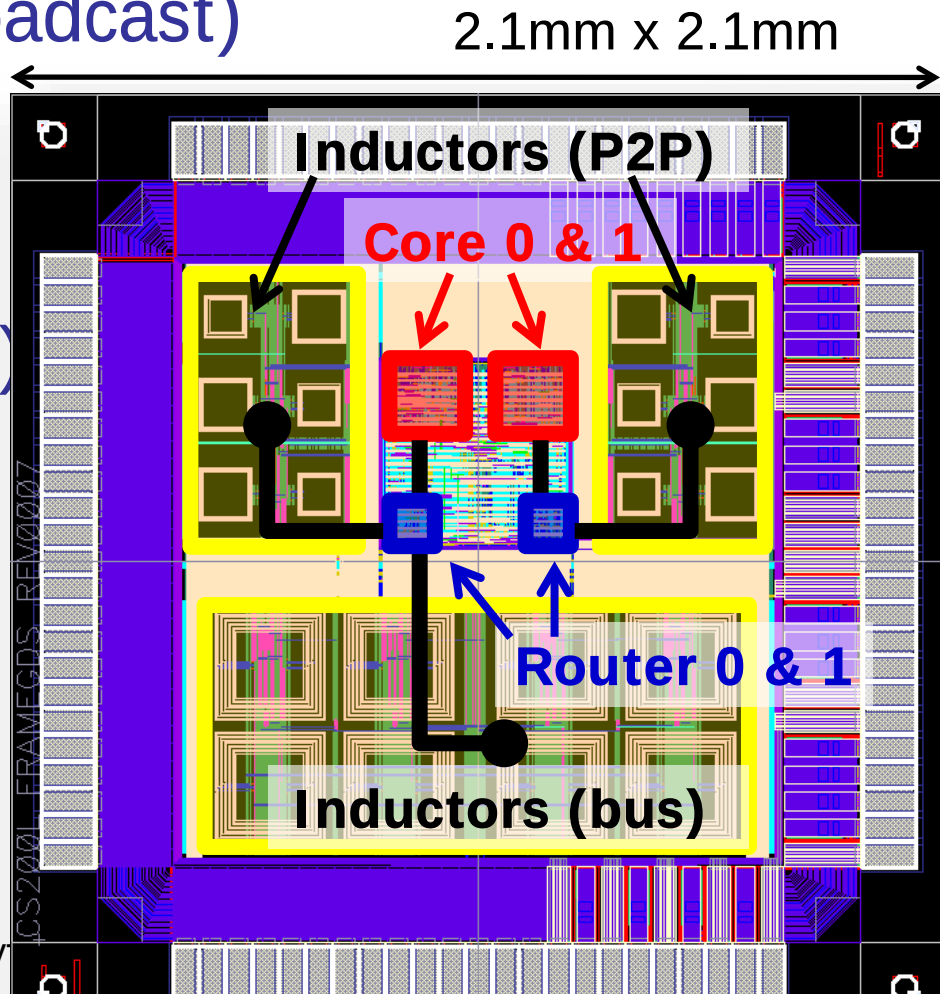
An example: Cube-0 (2010)

- Test chip for vertical communication schemes
  - Vertical point-to-point link between adjacent chips
  - Vertical shared bus (broadcast)

[Matsutani, NOCS'11]

- Each chip has
  - 2 cores (packet counter)
  - 2 routers
  - Inductors (P2P ring)
  - Inductors (vertical bus)

Process: Fujitsu 65nm (CS202SZ)
Voltage: 1.2V
System clock: 200MHz



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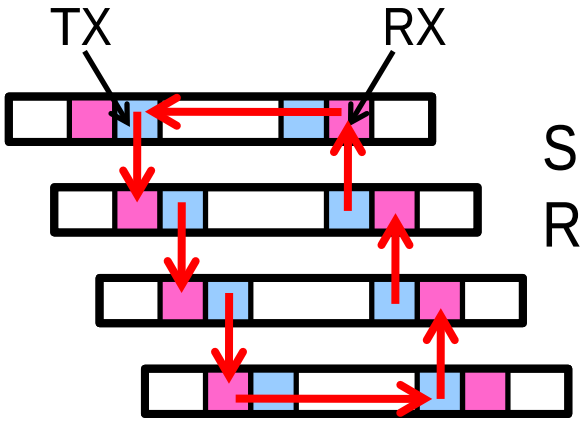
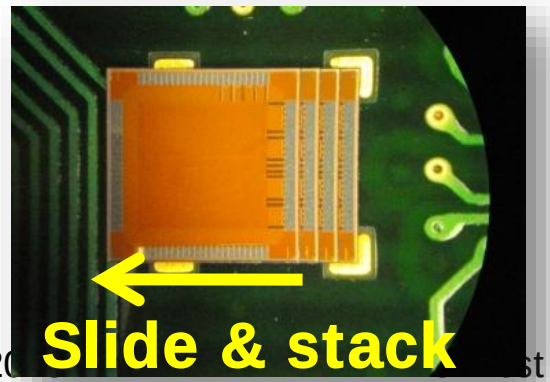
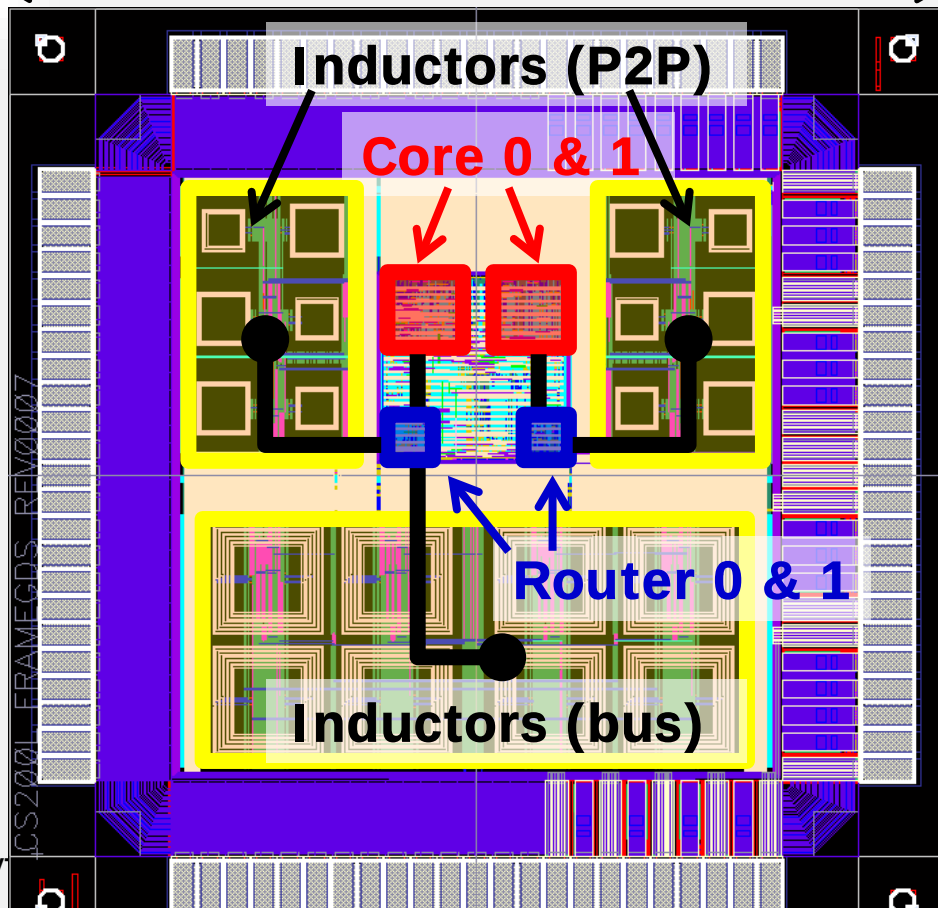


Stacking for Ring network



2.1mm x 2.1mm



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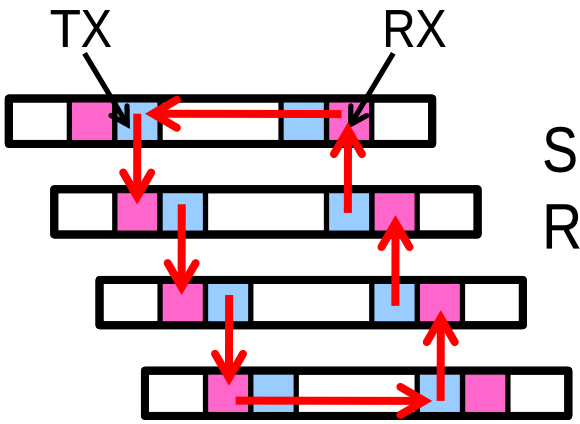

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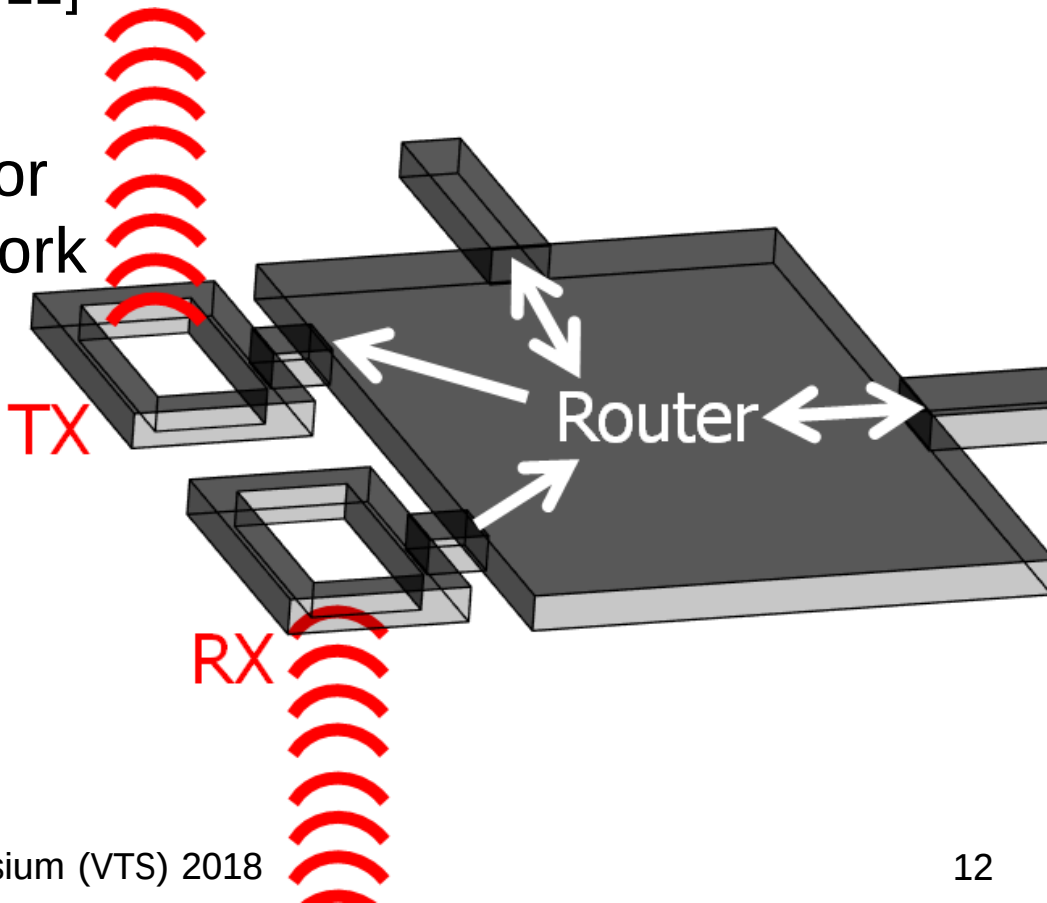
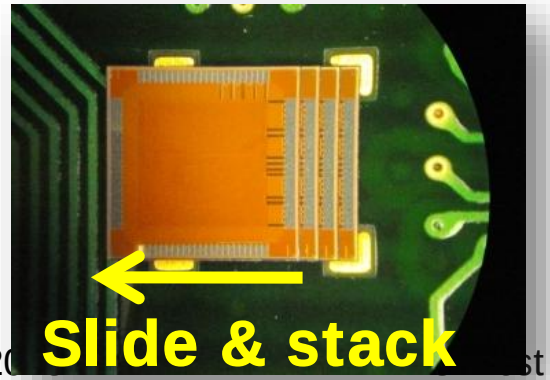


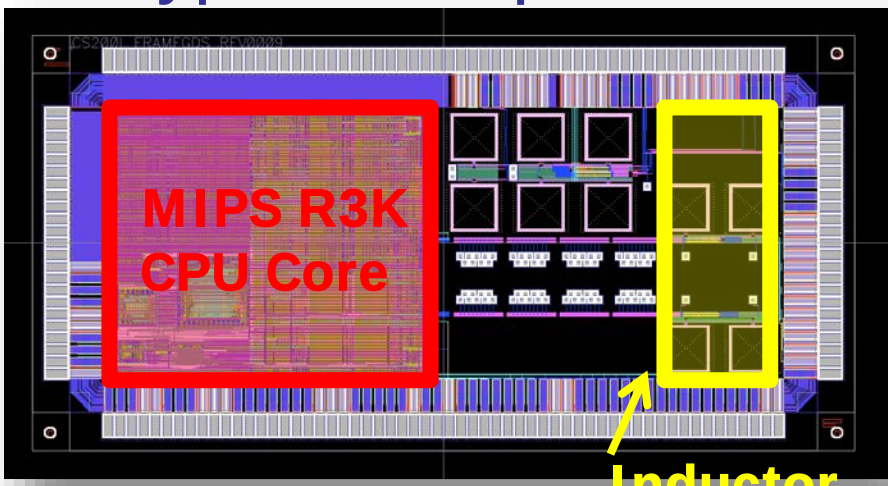


An example: Cube-1 (2012)

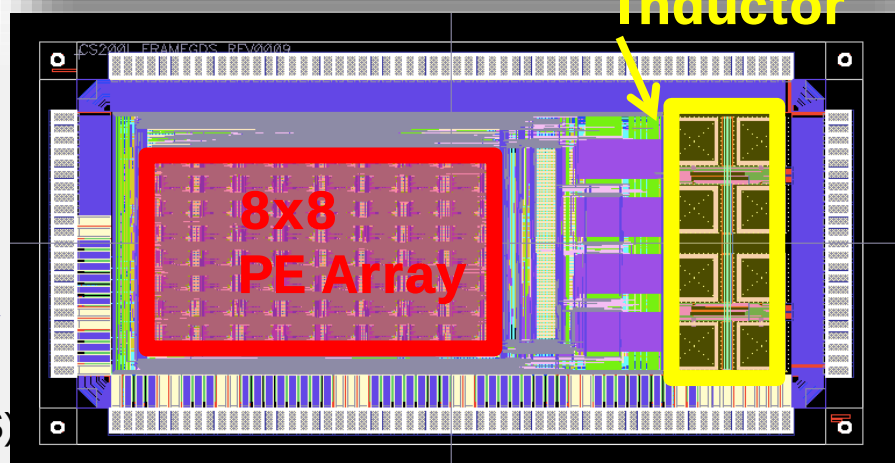
- Test chips for building-block 3D systems
  - Two chip types: Host CPU chip & Accelerator chip
  - We can customize number & types of chips in SiP

[Miura, IEEE Micro 13]

- Cube-1 Host CPU chip
  - Two 3D wireless routers
  - MIPS-like CPU

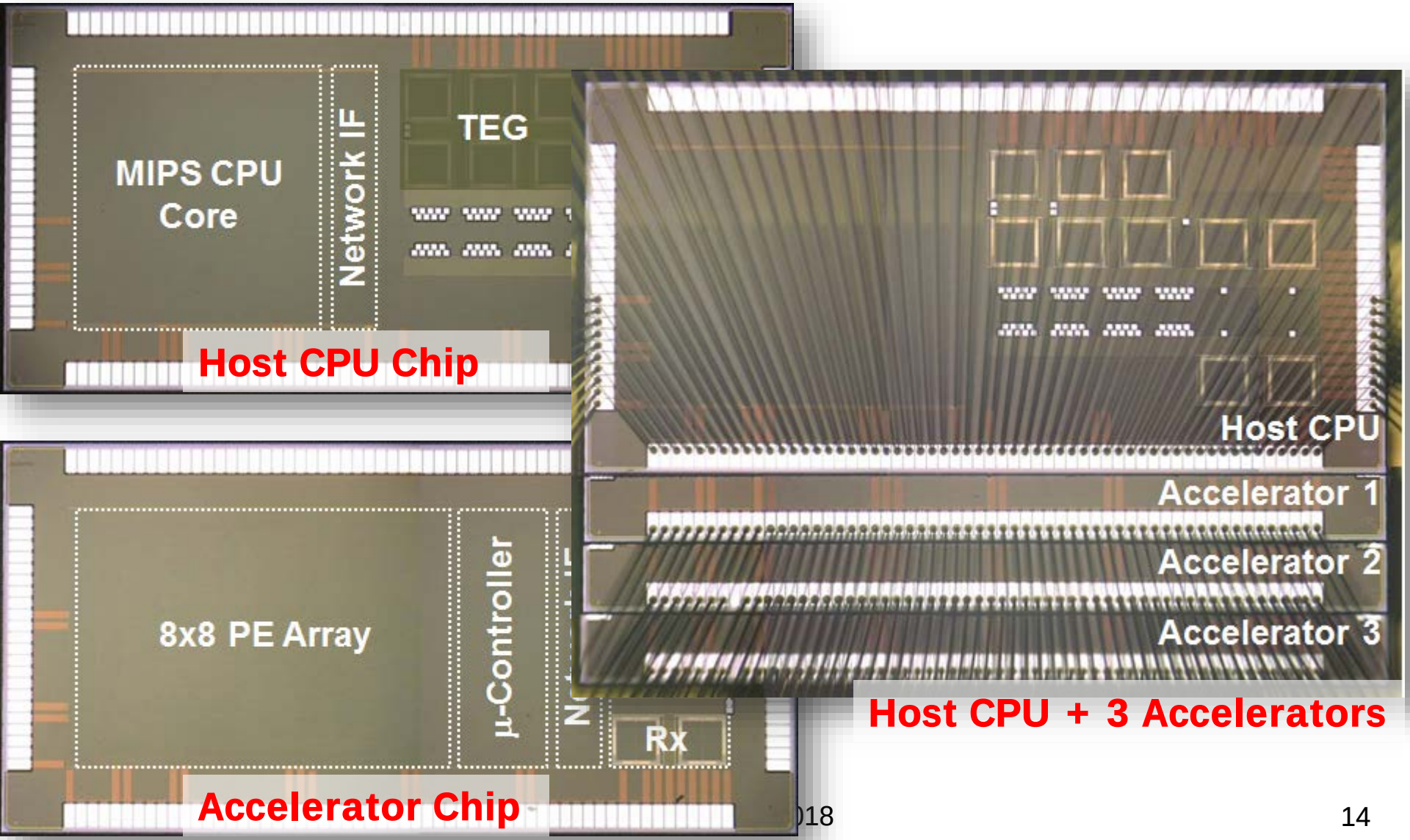


- Cube-1 Accelerator chip
  - Two 3D wireless routers
  - Processing element array



An example: Cube-1 (2012)

- Microphotographs of test chips [Miura, IEEE Micro 13]



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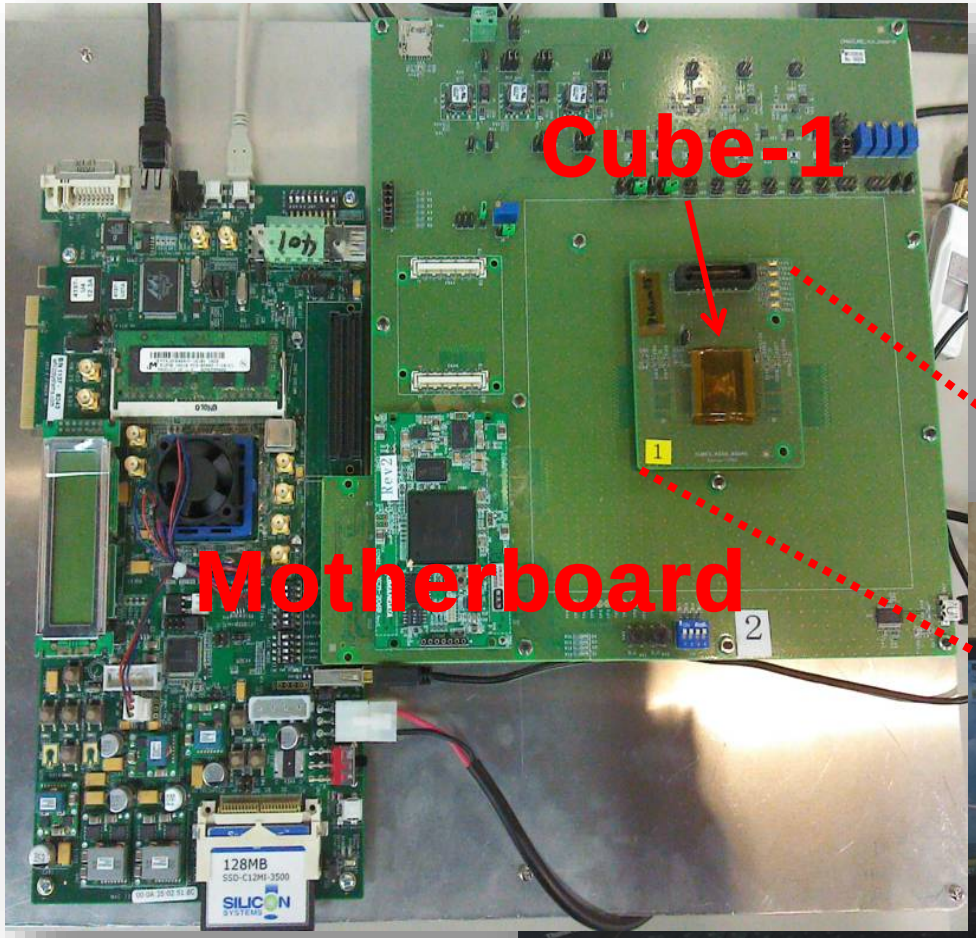
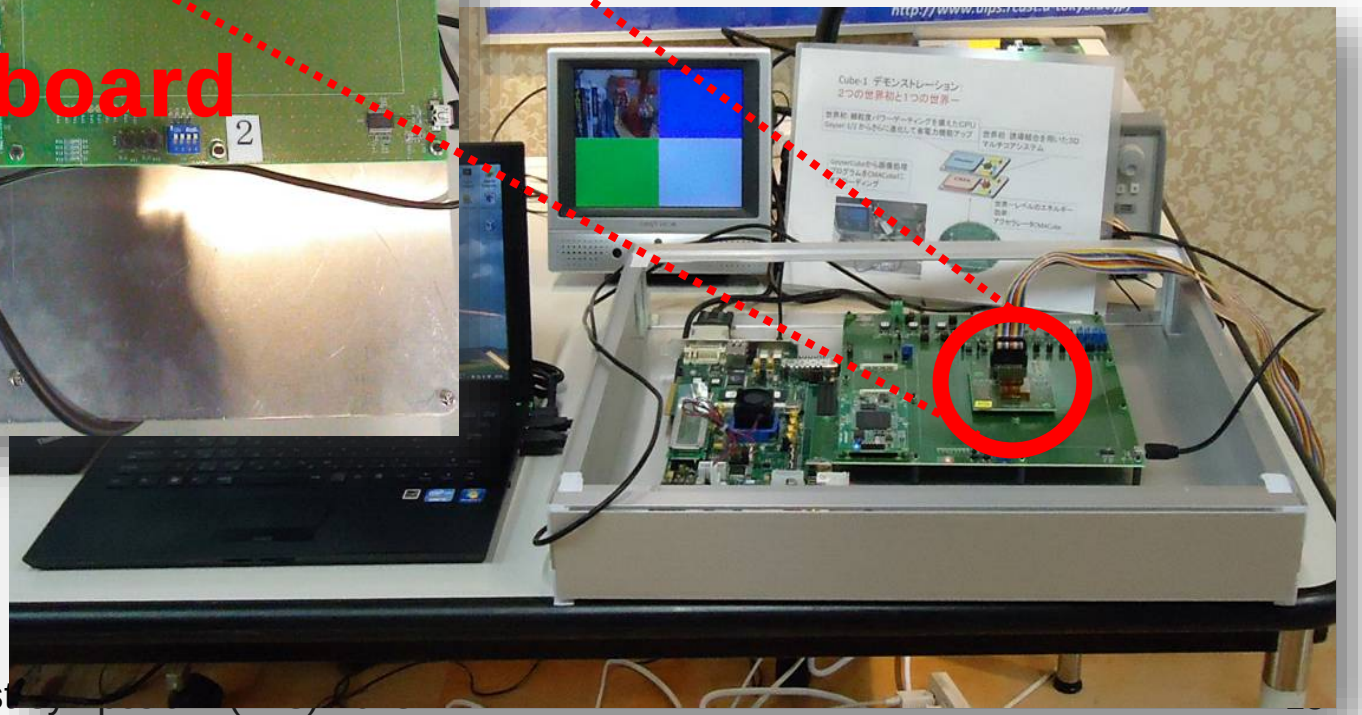


Cube-1 demo system

PE array chip performs image processing

CPU chip for control

[Miura, HotChips'13 Demo]



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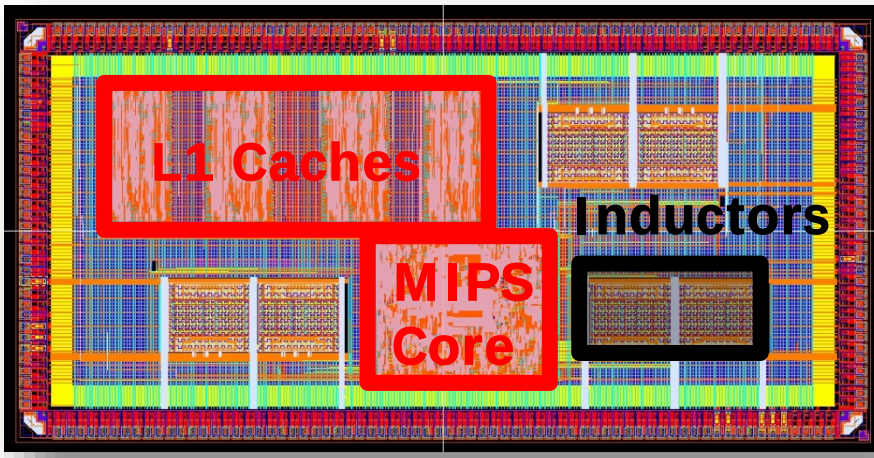
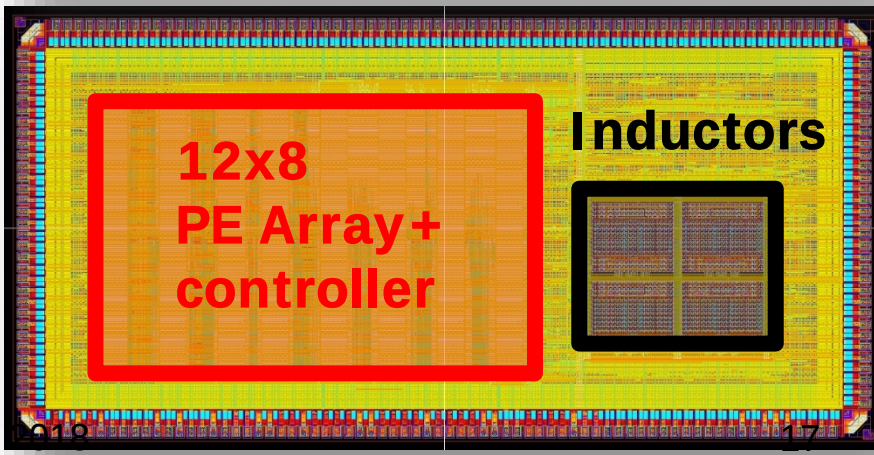
Current design: Cube-2 (2016)

- A practical building-block 3D systems
  - CPU chip, Accelerator chip, NN chip, and KVS chip
  - Renesas Electronics SOTB 65nm with Body biasing
- Cube-2 Host CPU chip
  - MIPS-like CPU
- Cube-2 Accelerator chip
  - Processing element array
- Cube-2 NN chip
  - Neural network prediction
- Cube-2 KVS chip
  - Key-value store w/ SRAM





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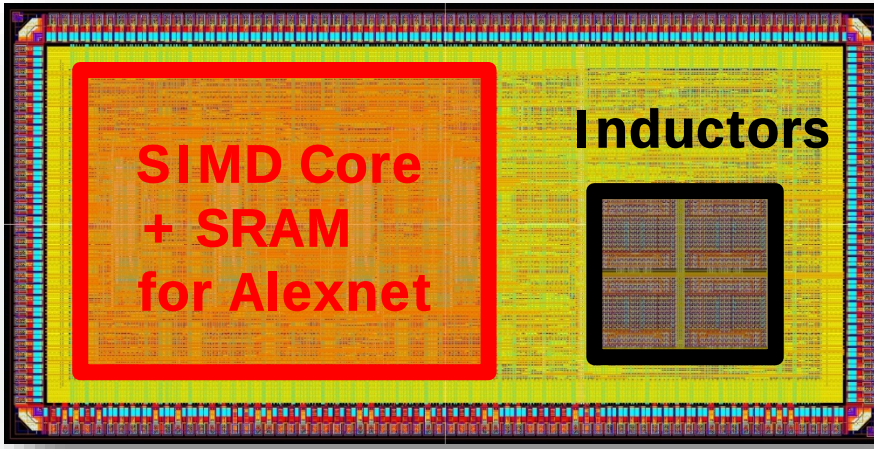
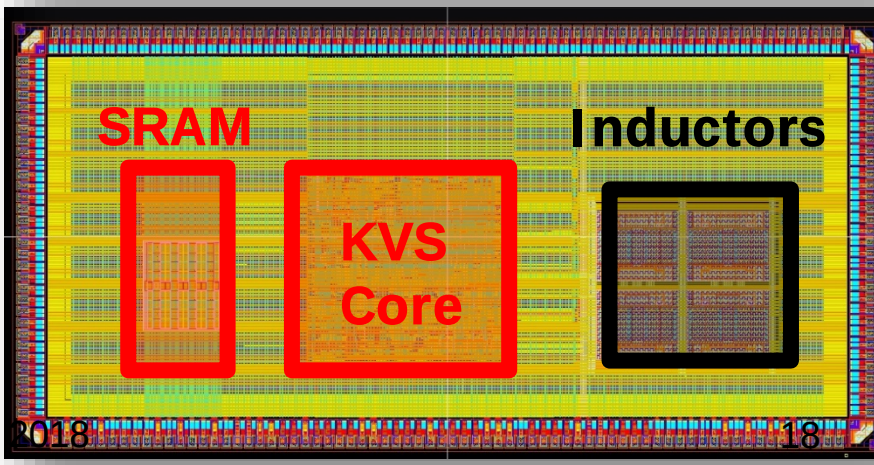
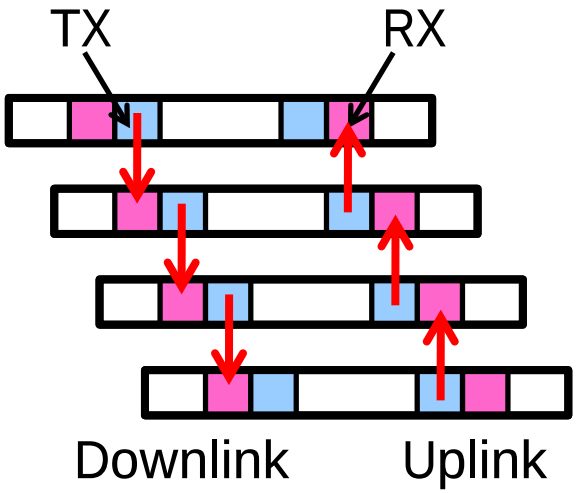
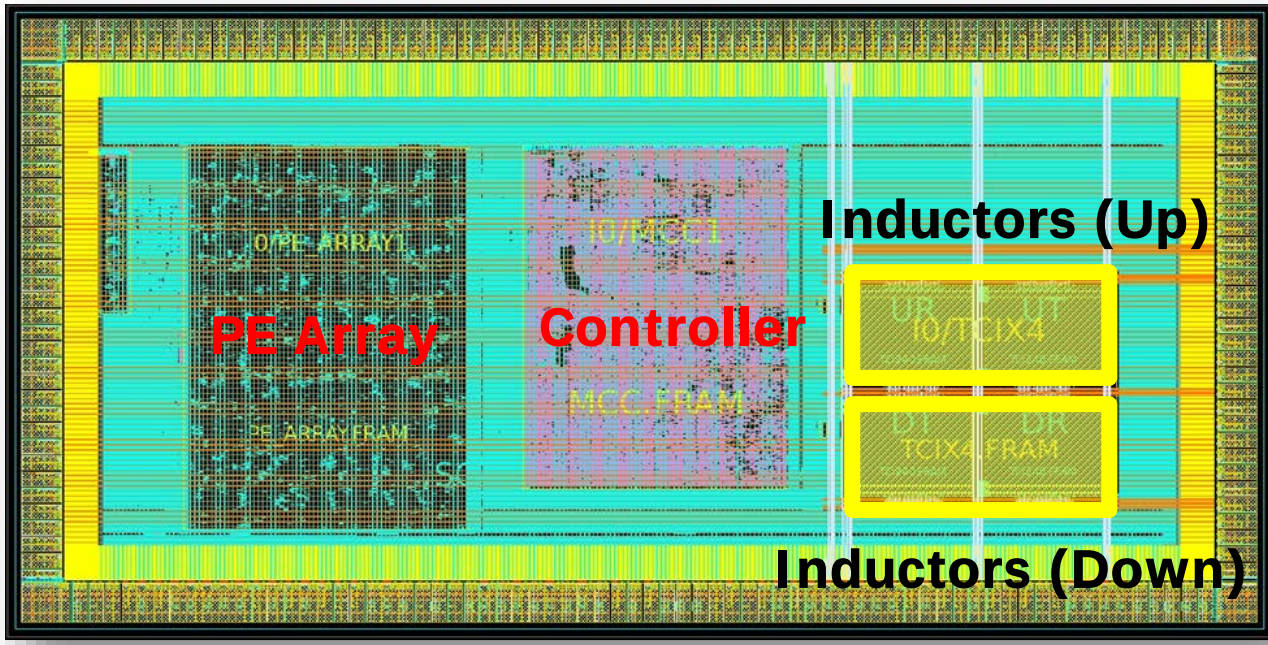




An example: Cube-2 (2016)

- Simpler vertical network for Cube-2
  - Vertical linear network (8 VCs)
  - Credit signal for flow control is piggybacked on packets on the opposite link





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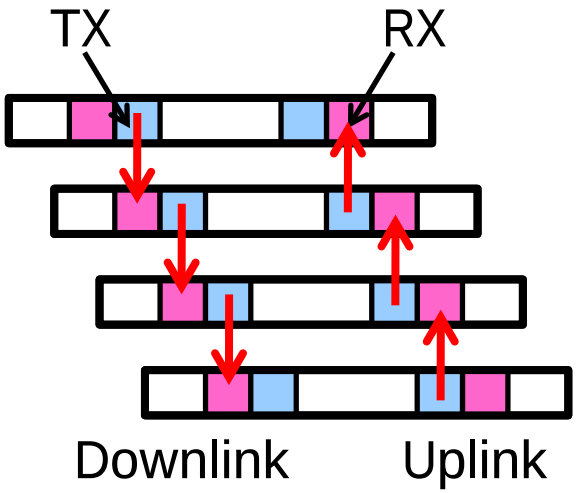

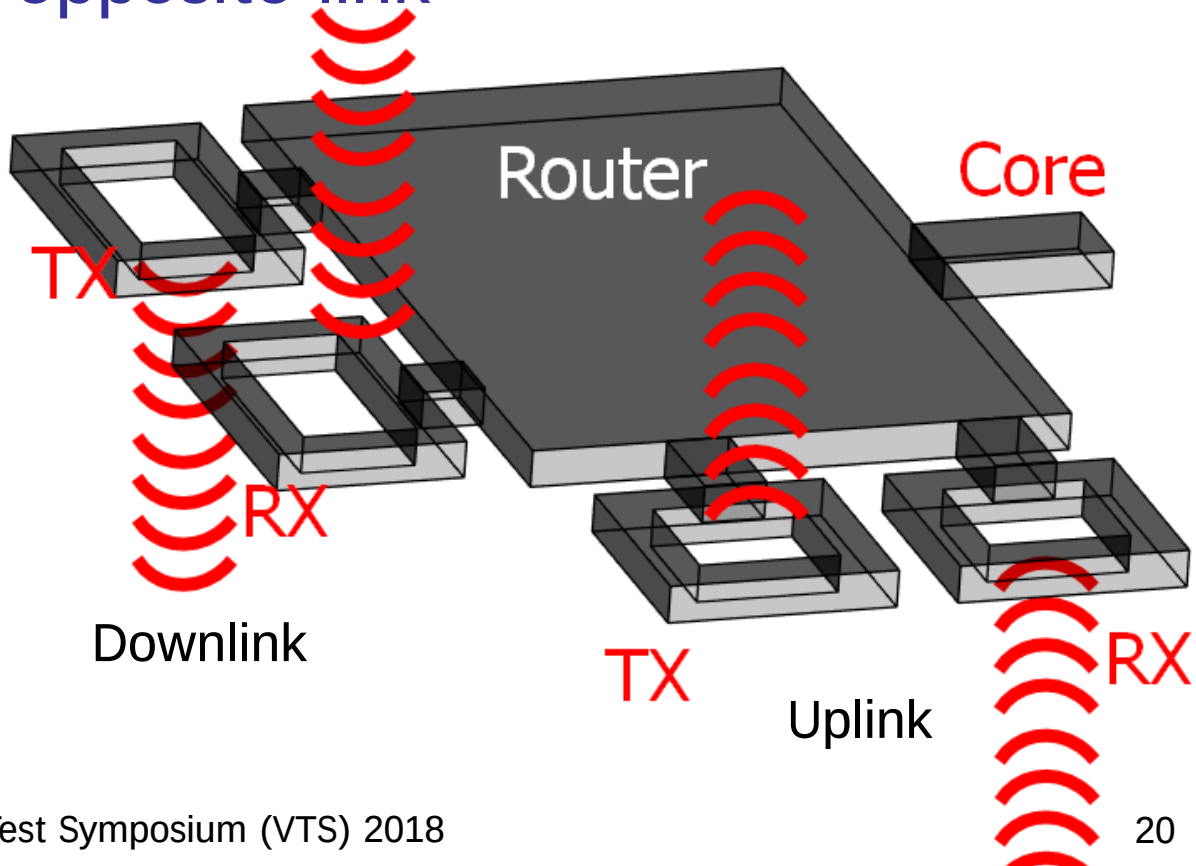

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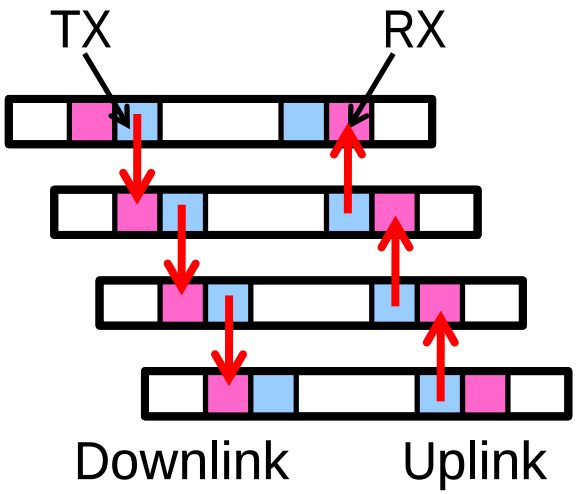

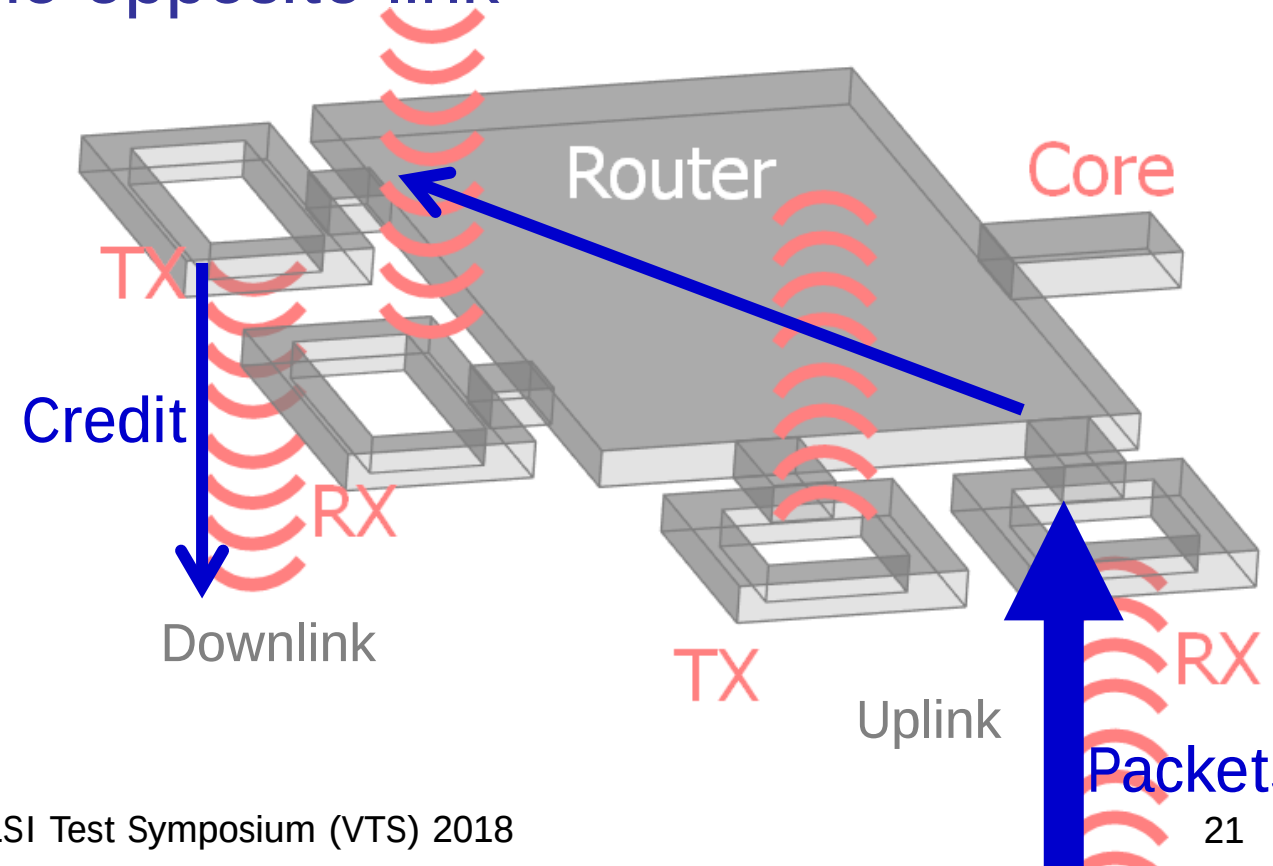

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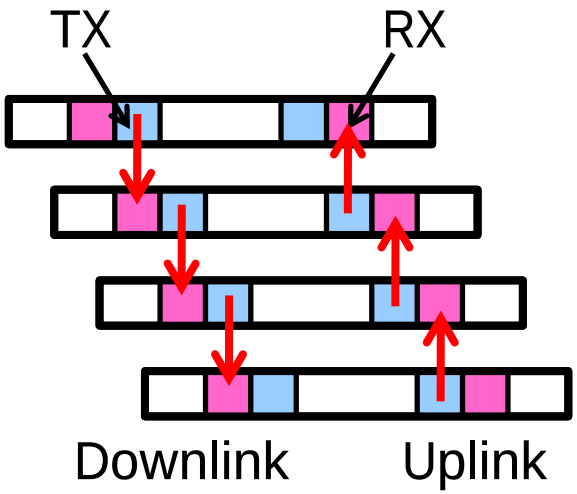
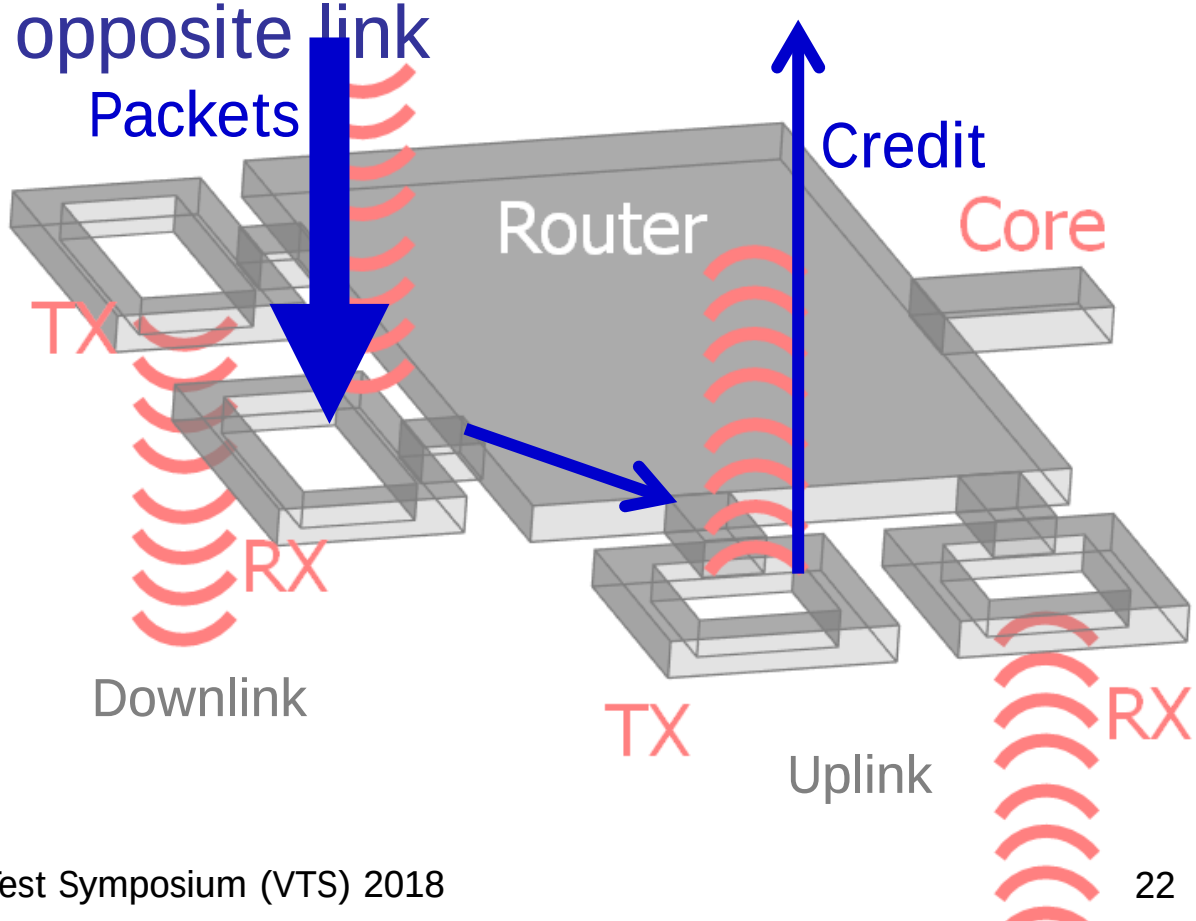
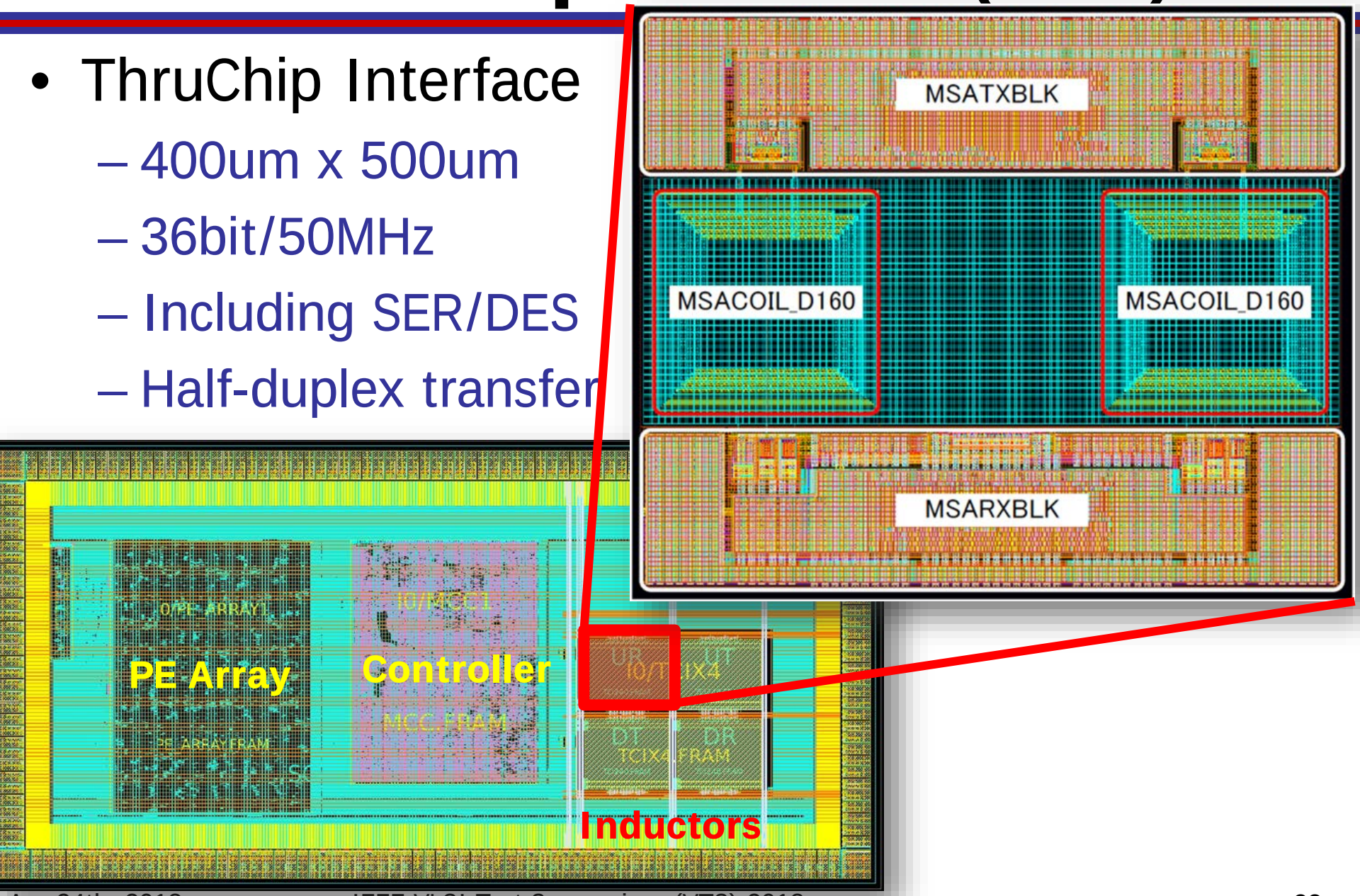




An example: Cube-2 (2016)

- ThruChip Interface
  - 400um x 500um
  - 36bit/50MHz
  - Including SER/DES
  - Half-duplex transfer



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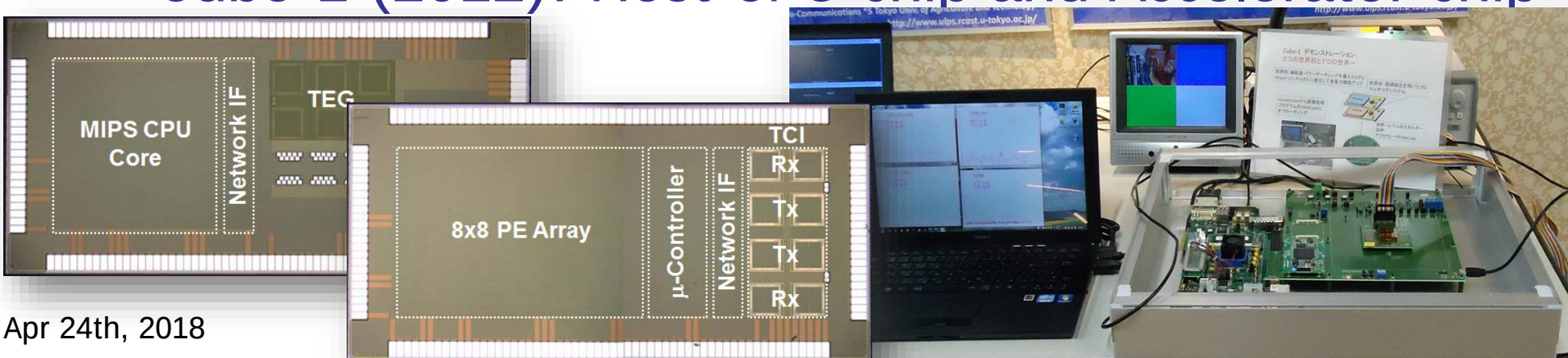
- Inductive-coupling 3D SiP
  - A low cost alternative to build low-volume custom systems by stacking off-the-shelf known-good-dies
  - No special process technology is required; inductors are implemented with metal layers
- Our history
  - Cube-0 (2010): Test (3D Wireless NoC only)
  - Cube-1 (2012): Host CPU chip and Accelerator chip



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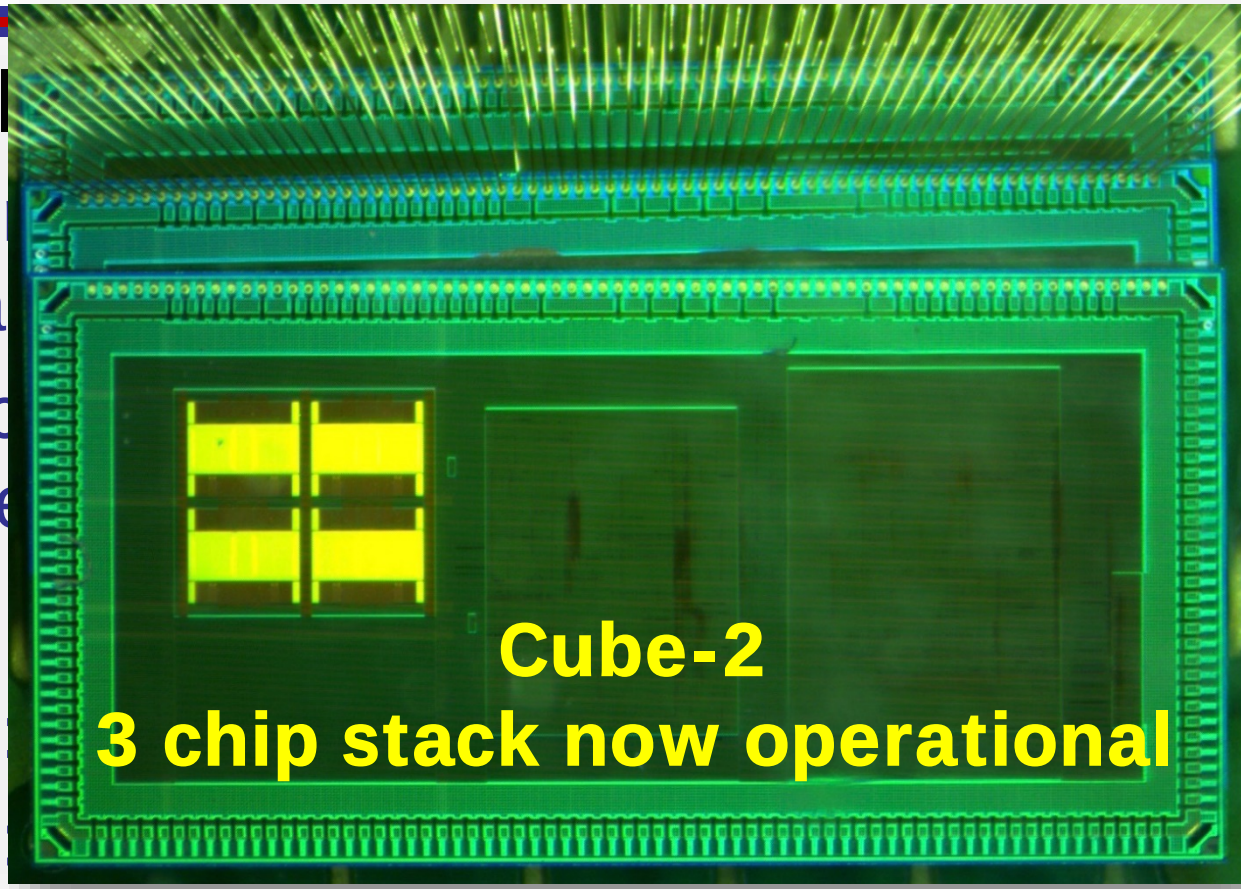

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  - T. Kagami, et.al., "Efficient 3-D Bus Architectures for Inductive-Coupling ThruChip Interfaces", IEEE Trans on VLSI (2015).